Chapter 6 MOSFET

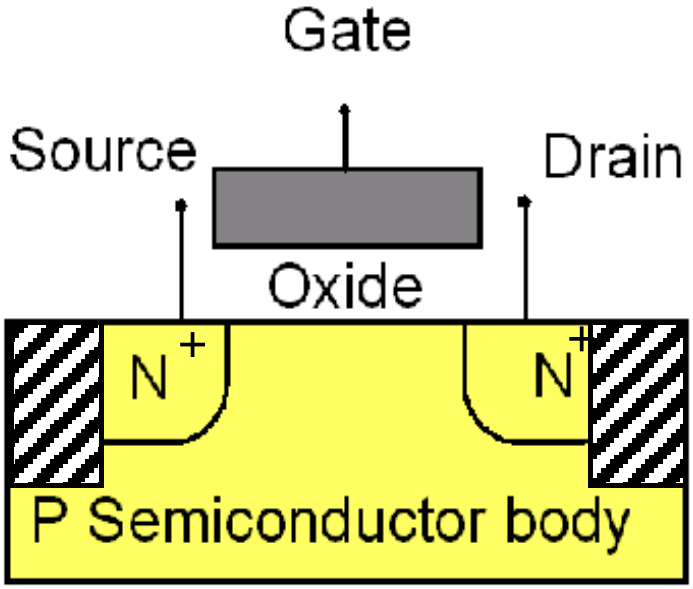
The MOSFET (MOS Field-Effect Transistor) is the building block of Gb memory chips, GHz microprocessors, analog, and RF circuits.

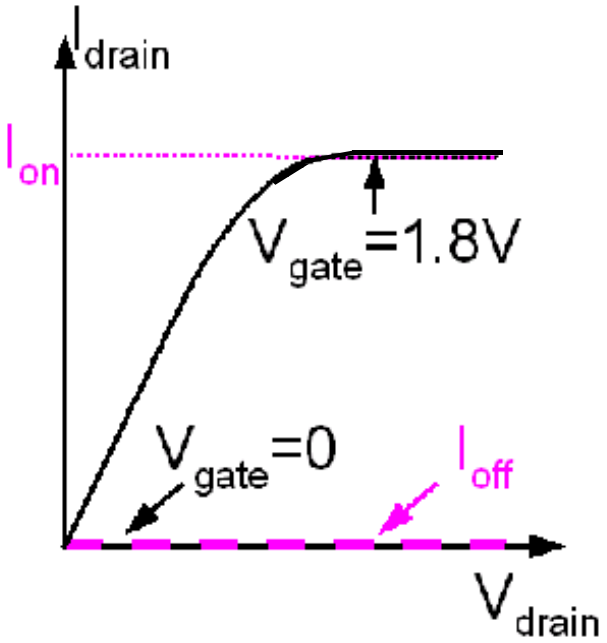
Match the following MOSFET characteristics with their applications:

- small size
- high speed
- low power
- high gain

6.1 Introduction to the MOSFET

Basic MOSFET structure and IV characteristics



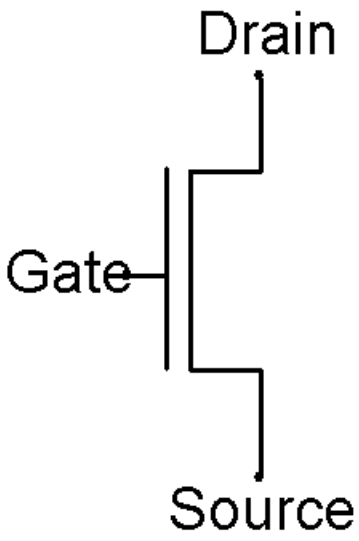


What is desirable: large I_{on}, small I_{off}

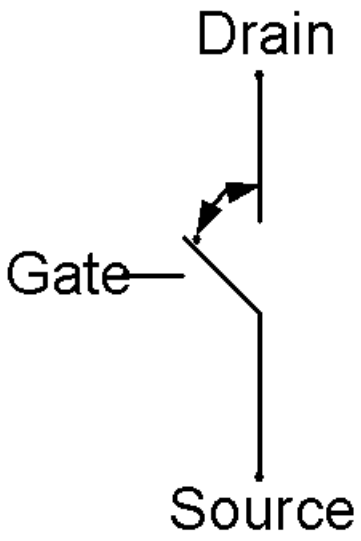
6.1 Introduction to the MOSFET

Two ways of representing a MOSFET:

Circuit Symbol



Simple Switch



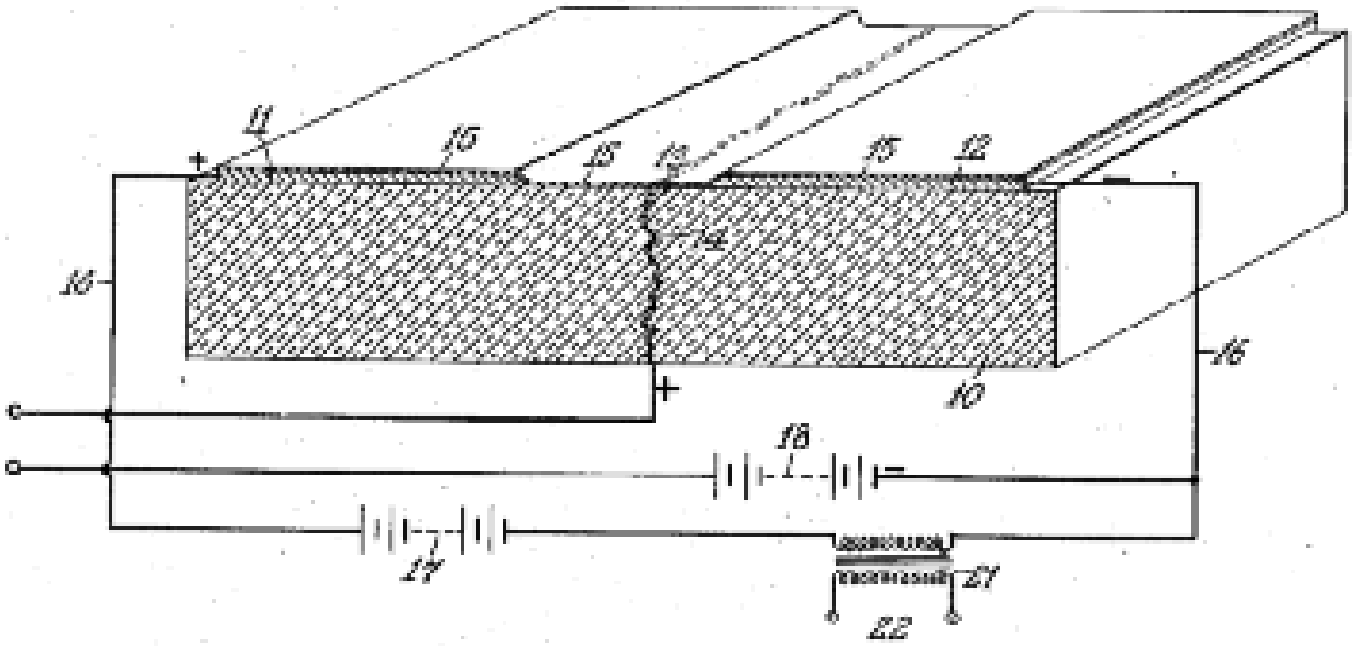
Early Patents on the Field-Effect Transistor

Jan. 28, 1930. J. E. LILIENFELD 1,745,175

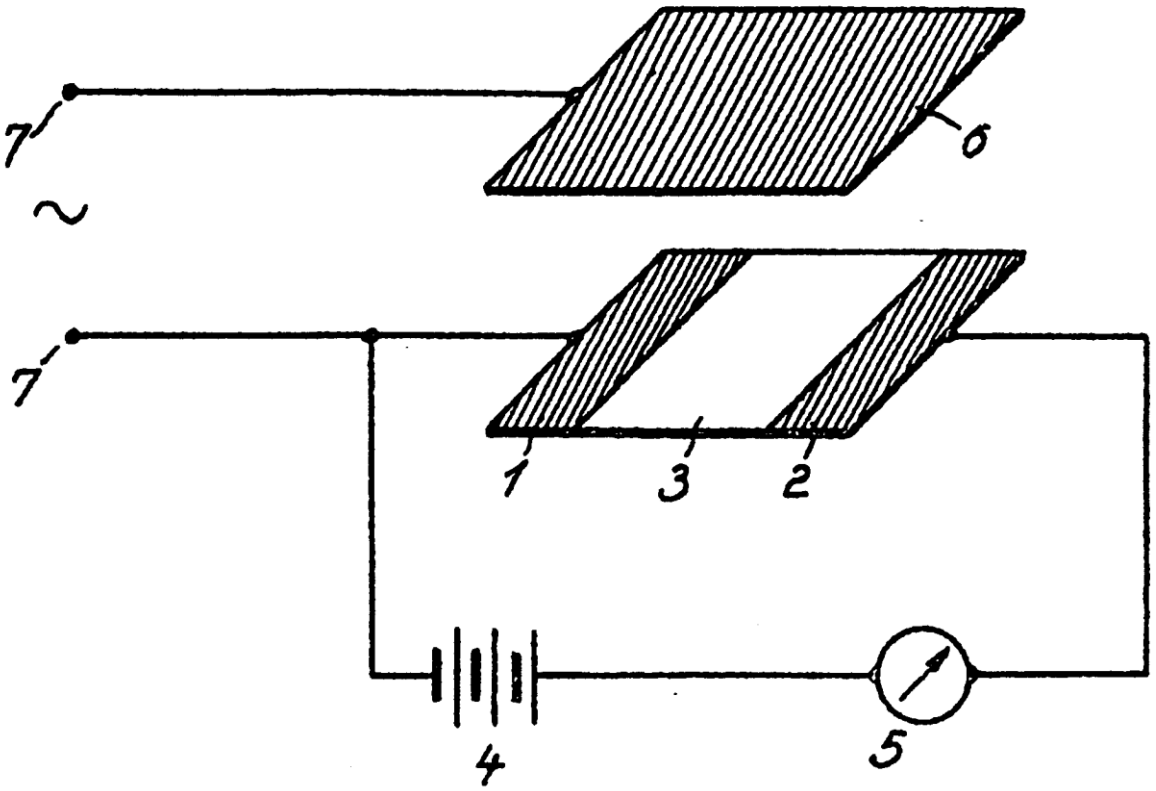
METHOD AND APPARATUS FOR CONTROLLING ELECTRIC CURRENTS

Filed Oct. 8, 1926

Fig. 1.



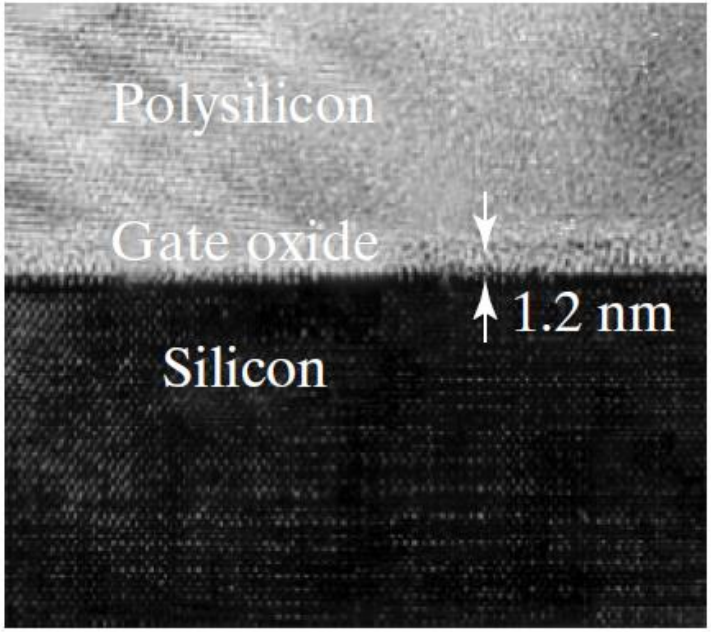
Early Patents on the Field-Effect Transistor



In 1935, a British patent was issued to Oskar Heil.
A working MOSFET was not demonstrated until 1955.
Using today's terminology, what are 1, 2, and 6?

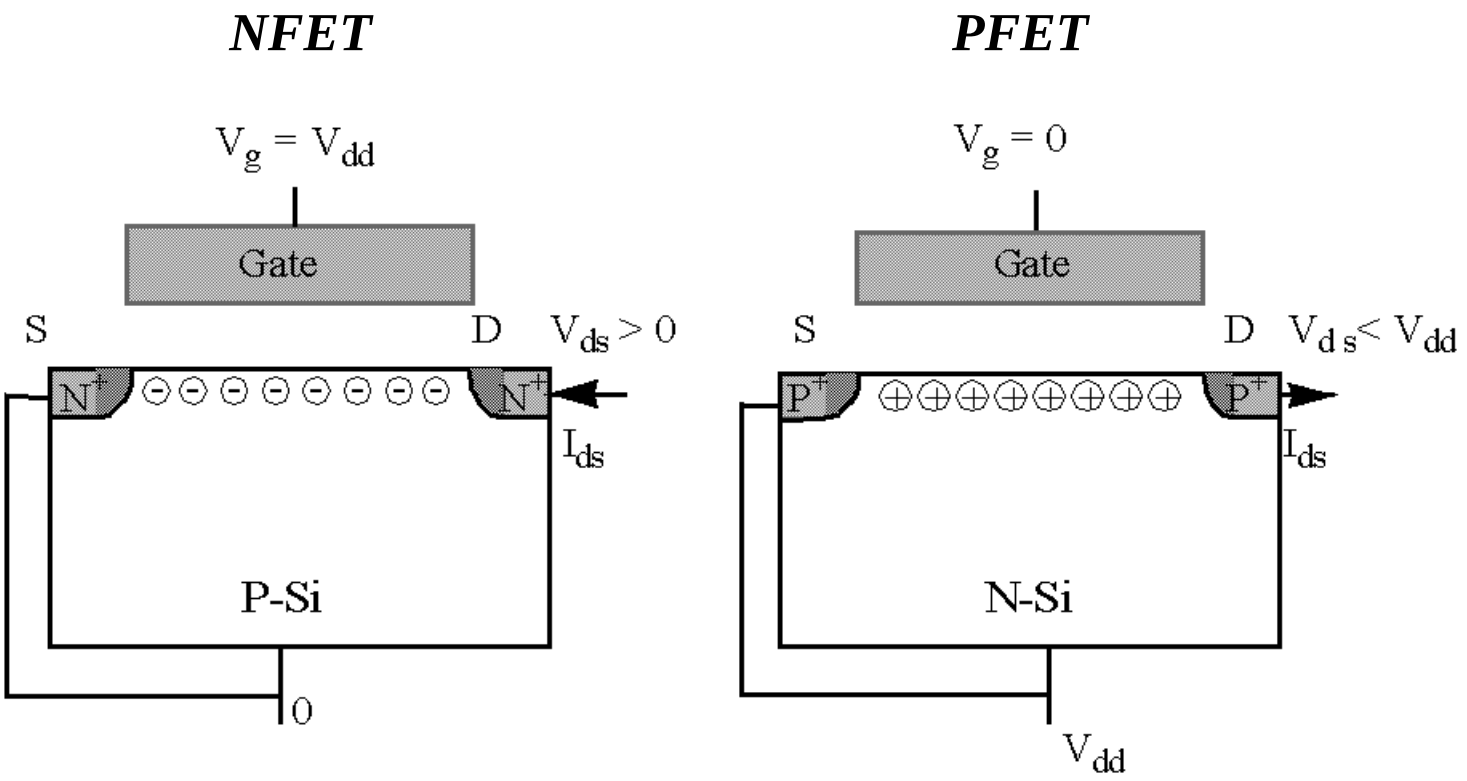
6.2 MOSFETs Technology

Polysilicon gate and 1.2nm SiO_2



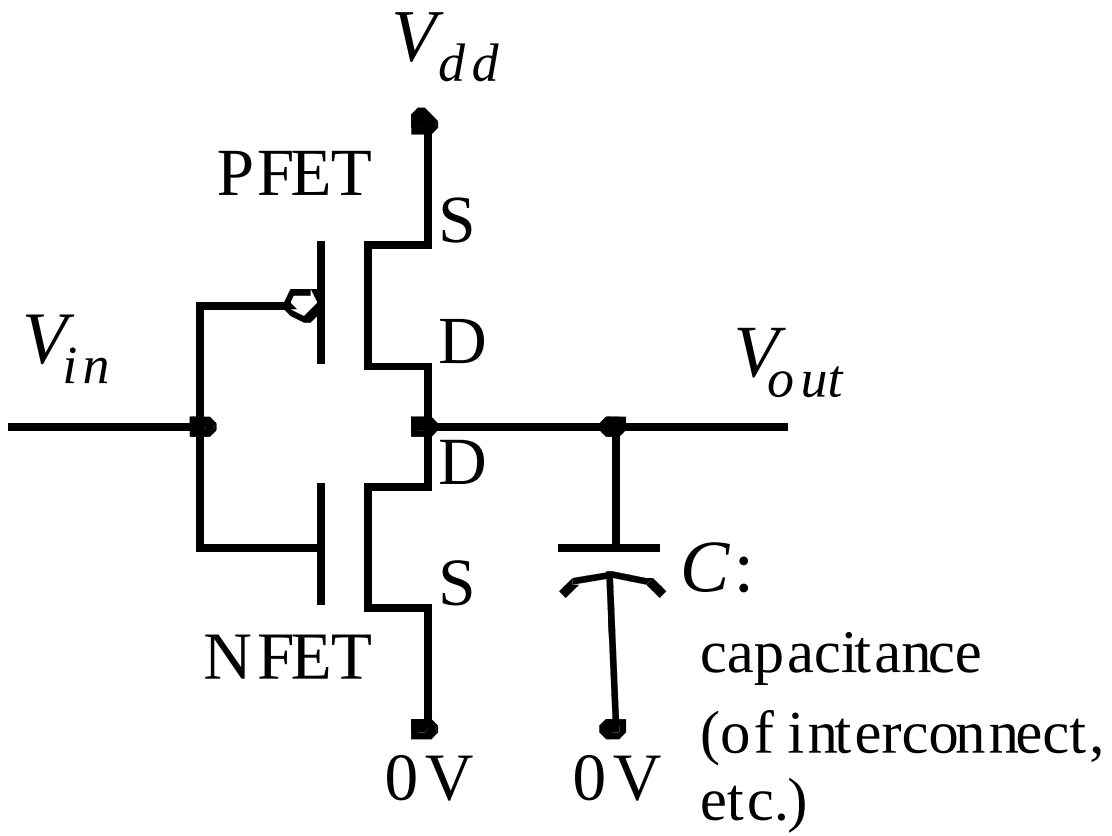
- 1.2 nm SiO_2 used in production. Leakage current through the oxide limits further thickness reduction.

6.2 Complementary MOSFETs Technology



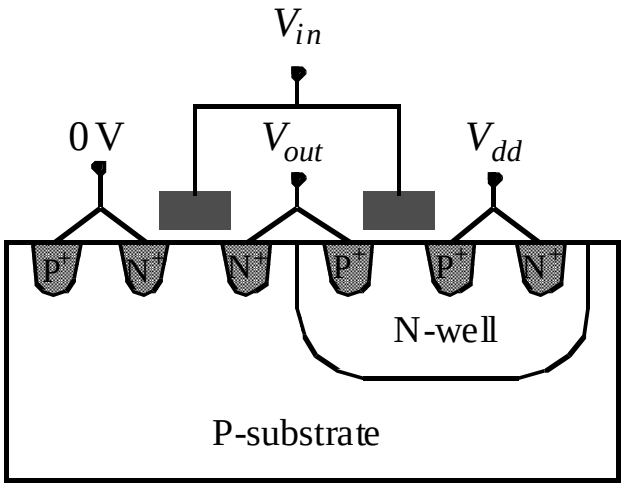
When $V_g = V_{dd}$, the NFET is on and the PFET is off.
When $V_g = 0$, the PFET is on and the NFET is off.

CMOS (Complementary MOS) Inverter

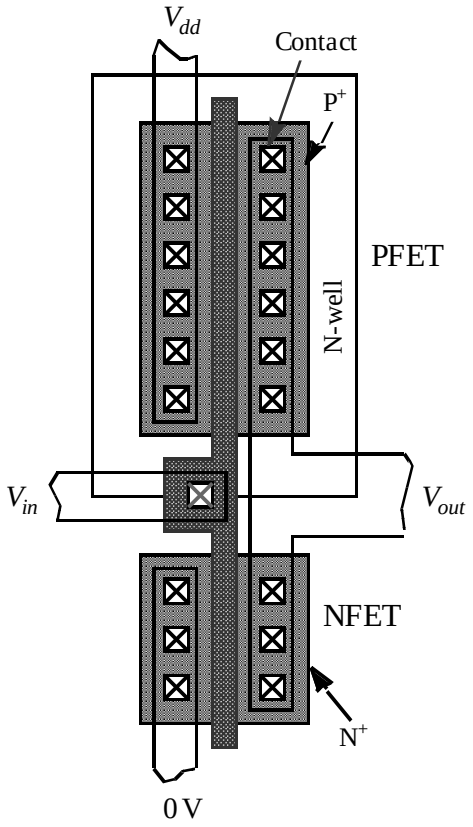


A CMOS inverter is made of a PFET ***pull-up device*** and a NFET ***pull-down device***. V_{out} = ? if V_{in} = 0 V.

CMOS (Complementary MOS) Inverter



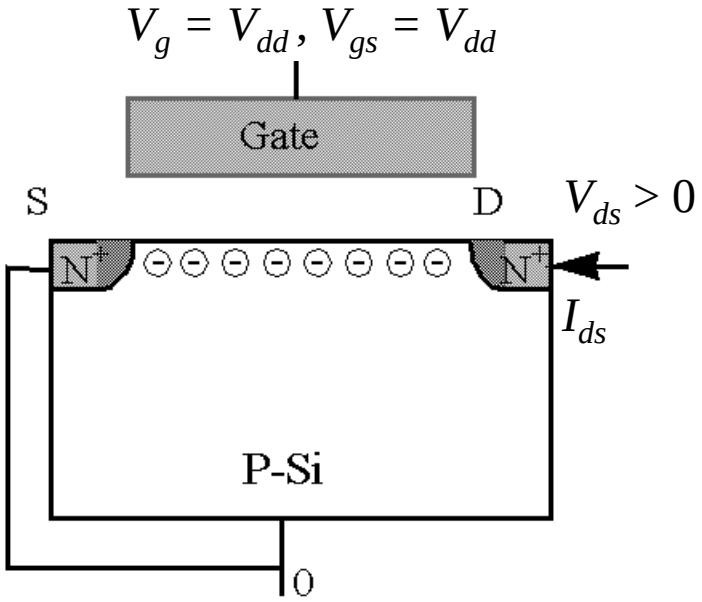
• NFET and PFET can be fabricated on the same chip.



• basic layout of a CMOS inverter

6.3 Surface Mobilities and High-Mobility FETs

6.3.1 Surface Mobilities



How to measure the surface mobility:

$$I_{ds} = W \times Q_{inv} \times v = W Q_{inv} \mu_{ns} \mathcal{E} = W Q_{inv} \mu_{ns} V_{ds} / L$$

$$= W C_{oxe} (V_{gs} - V_t) \mu_{ns} V_{ds} / L$$

Mobility is a function of the average of the fields at the bottom and the top of the inversion charge layer, $\mathcal{E}_b$ and $\mathcal{E}_t$.

From Gauss's Law,

$$\mathcal{E}_b = -Q_{dep}/\varepsilon_s$$

$$V_t = V_{fb} + \phi_{st} - Q_{dep}/C_{oxe}$$

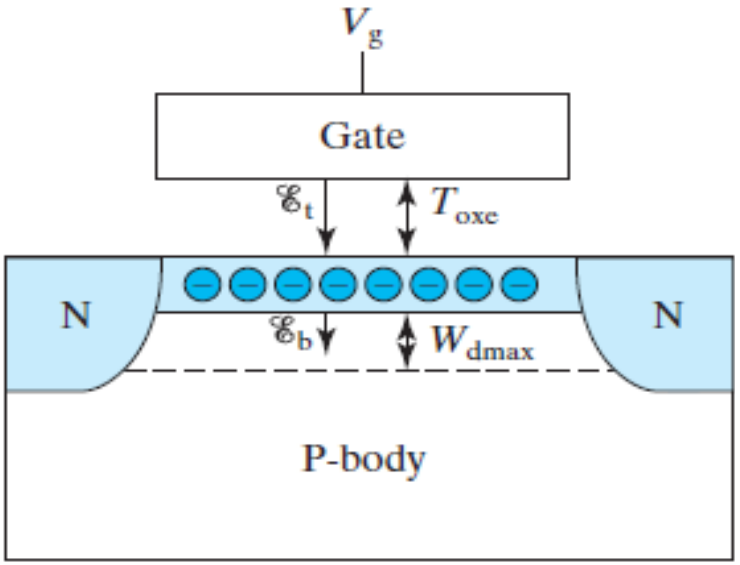
Therefore,

$$\mathcal{E}_b = \frac{C_{oxe}}{\varepsilon_s}(V_t - V_{fb} - \phi_{st})$$

$$\mathcal{E}_t = -(Q_{dep} + Q_{inv})/\varepsilon_s$$

$$= \mathcal{E}_b - Q_{inv}/\varepsilon_s = \mathcal{E}_b + \frac{C_{oxe}}{\varepsilon_s}(V_{gs} - V_t)$$

$$= \frac{C_{oxe}}{\varepsilon_s}(V_{gs} - V_{fb} - \phi_{st})$$

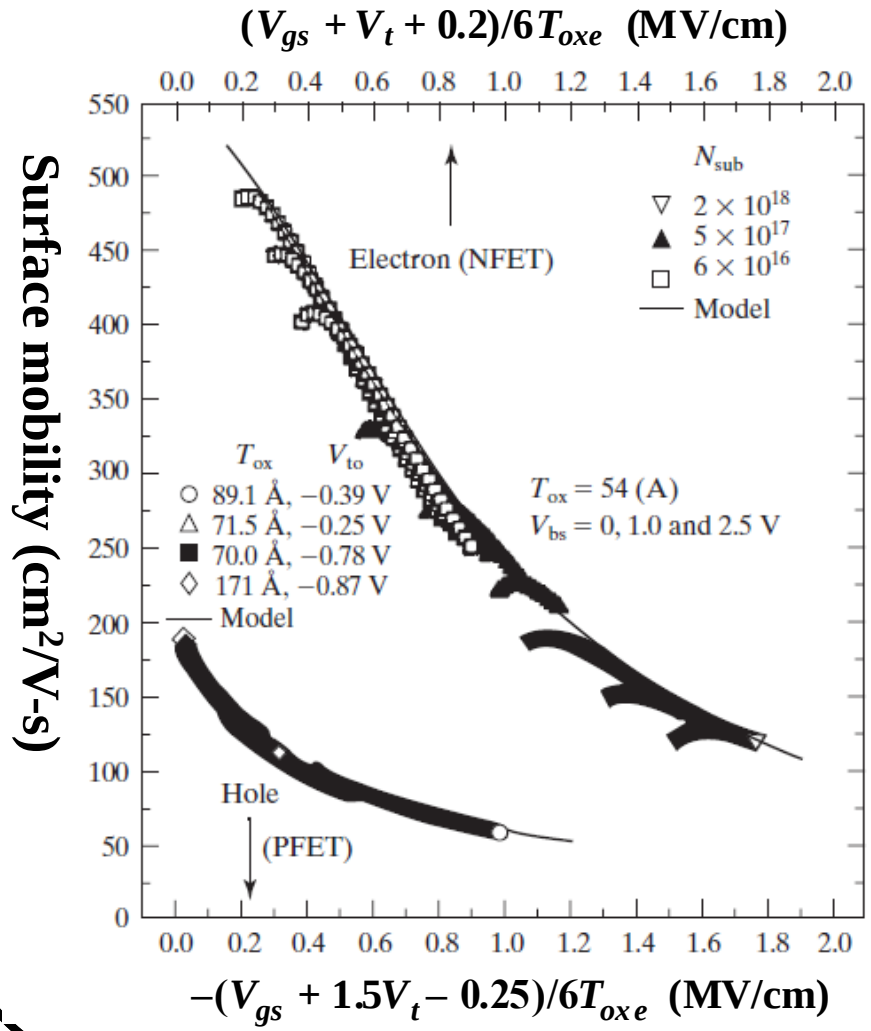


$$\therefore \frac{1}{2}(\mathcal{E}_b + \mathcal{E}_t) = \frac{C_{oxe}}{2\varepsilon_s}(V_{gs} + V_t - 2V_{fb} - 2\phi_{st})$$

$$\approx \frac{C_{oxe}}{2\varepsilon_s}(V_{gs} + V_t + 0.2\,\mathrm{V})$$

$$= \frac{V_{gs} + V_t + 0.2\,\mathrm{V}}{6T_{oxe}}$$

Universal Surface Mobilities



- Surface roughness scattering is stronger (mobility is lower) at higher V_g, higher V_t, and thinner T_{oxe}.

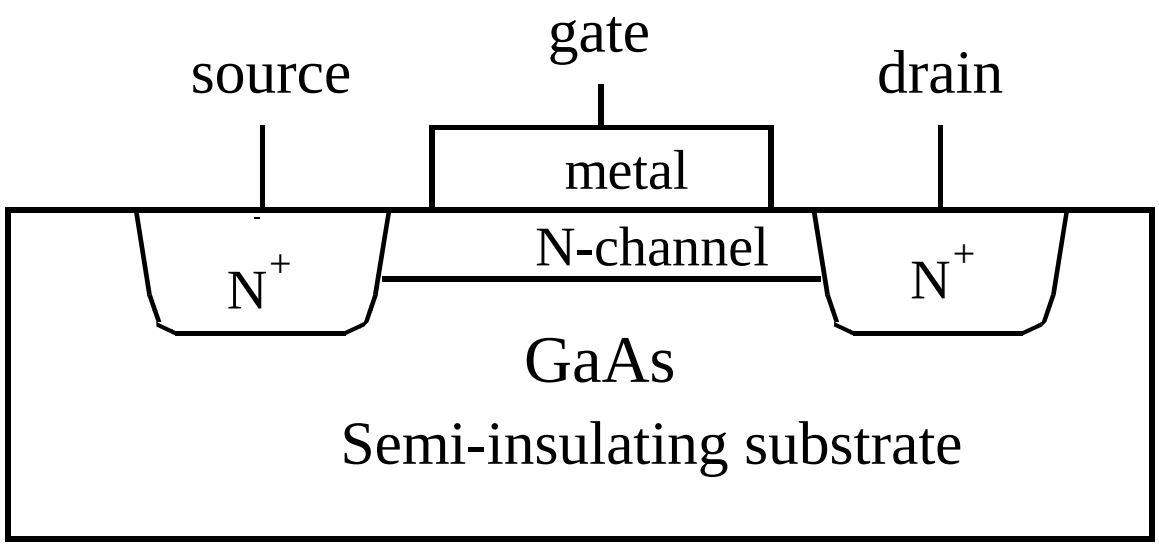
EXAMPLE: *What is the surface mobility at V_{gs}=1 V in an N-channel MOSFET with V_t=0.3 V and T_{oxe}=2 nm?*

Solution:

$$(V_{gs} + V_t + 0.2)/6T_{oxe}$$
$$= 1.5\,\text{V}/12\times10^{-7}\,\text{cm}$$
$$= 1.25\,\text{MV/cm}$$

1 MV is a megavolt (10^6 V). From the mobility figure, μ_{ns}=190 cm2/Vs, which is several times smaller than the bulk mobility.

6.3.2 GaAs MESFET

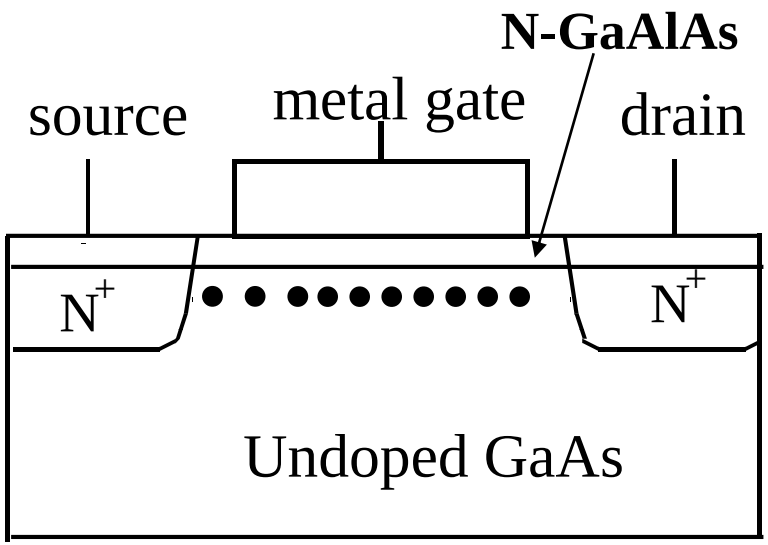


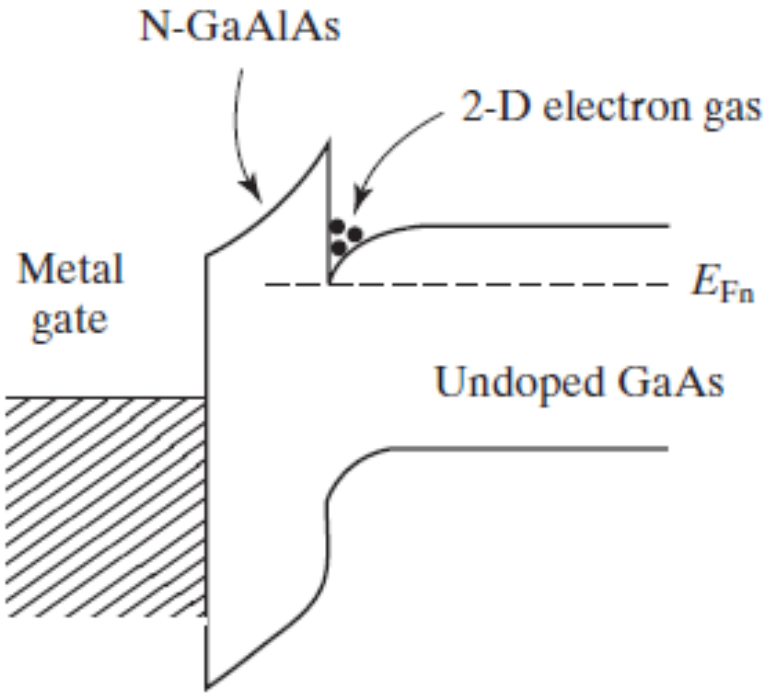
MESFET IV characteristics are similar to MOSFET's but does not require a gate oxide.

Question: What is the advantage of GaAs FET over Si FET?

Terms: ***depletion-mode transistor, enhancement-mode transistor***

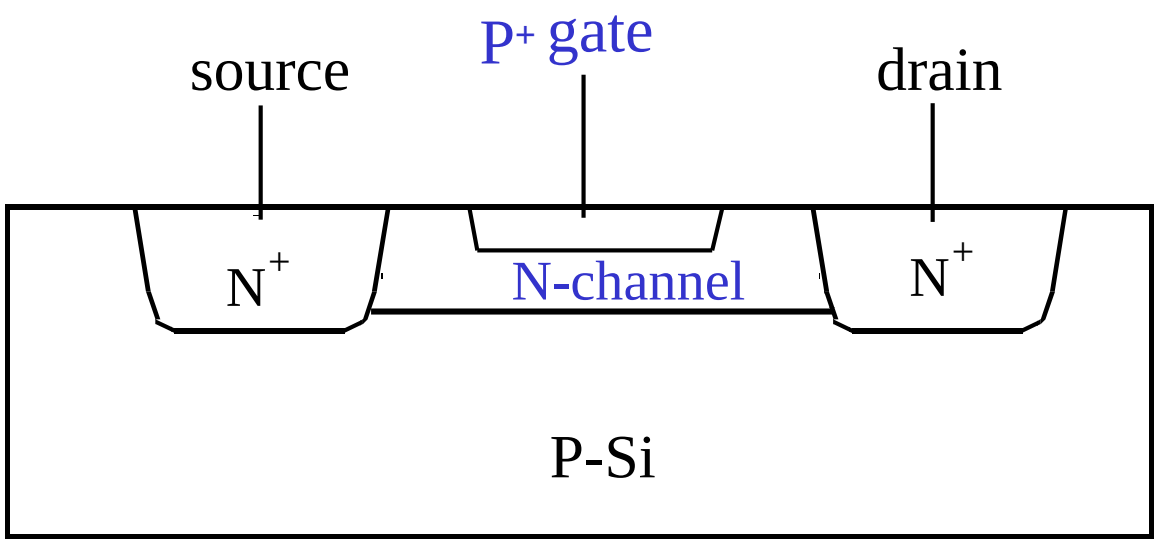
6.3.3 HEMT, High Electron Mobility Transistor





- A large-Eg semiconductor serves as the "gate dielectric".
- The layer of electrons is called **2D-electron-gas**, the equivalent of the inversion or accumulation layer of a MOSFET.

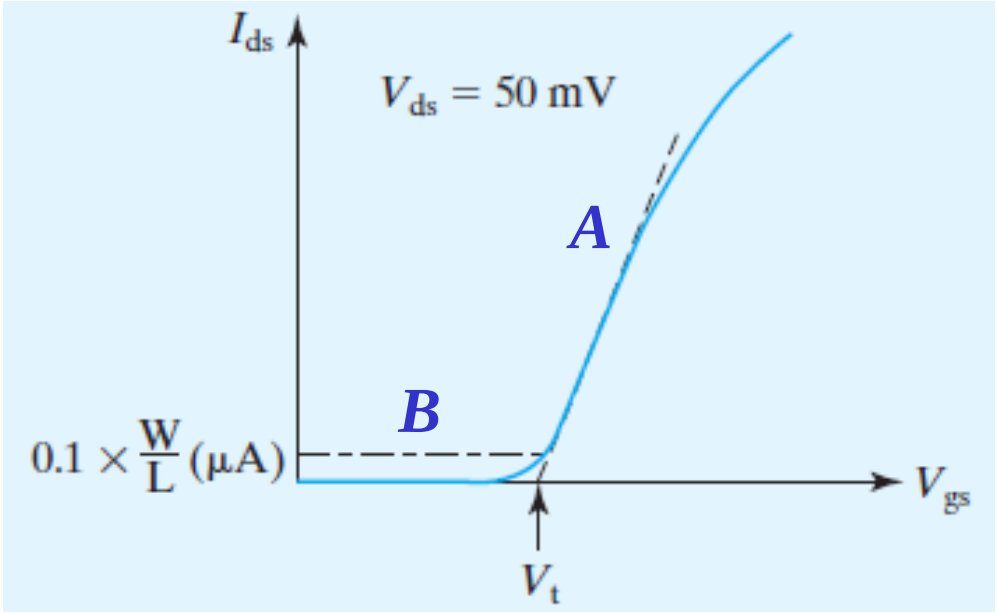
6.3.4 JFET



- The gate is a P^+N junction.
- The FET is a **junction field-effect transistor (JFET)**.

6.4 V_t and Body Effect

How to Measure the V_t of a MOSFET



- *Method A*. V_t is measured by extrapolating the I_{ds} versus V_{gs} curve to $I_{ds} = 0$.

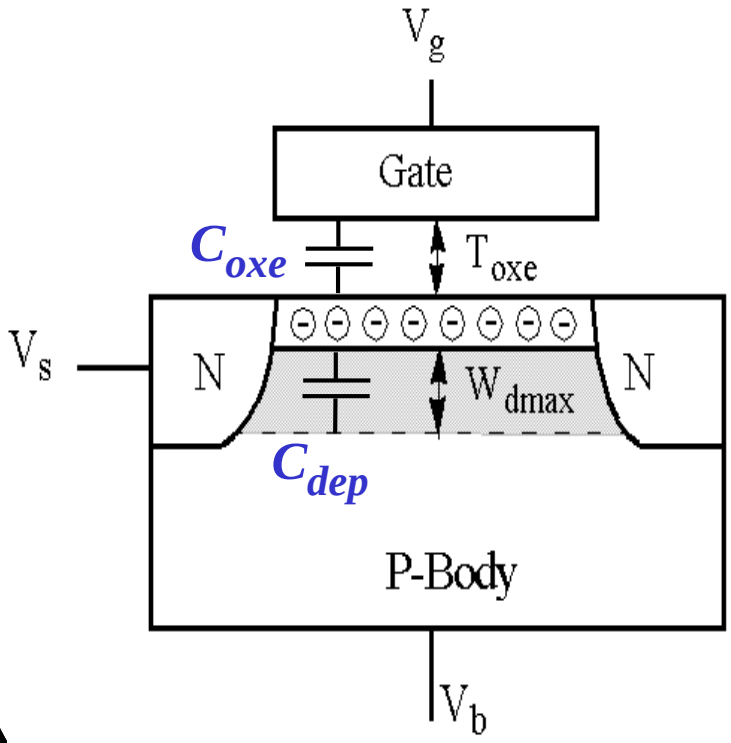
$$I_{dsat} = \frac{W}{L} C_{oxe}(V_{gs} - V_t)\mu_{ns} V_{ds} \propto V_{gs} - V_t$$

- *Method B*. The Vg at which $Ids = 0.1\mu A \times W/L$

MOSFET V_t and the Body Effect

- **Two capacitors => two charge components**

$$C_{dep} = \frac{\varepsilon_s}{W_{d\,\max}}$$



$$Q_{inv} = -C_{oxe}(V_{gs} - V_t) + C_{dep}V_{sb}$$

$$= -C_{oxe}(V_{gs} - (V_t + \frac{C_{dep}}{C_{oxe}}V_{sb}))$$

- Redefine V_t as

$$V_t(V_{sb}) = V_{t0} + \frac{C_{dep}}{C_{oxe}}V_{sb} = V_{t0} + \alpha V_{sb}$$

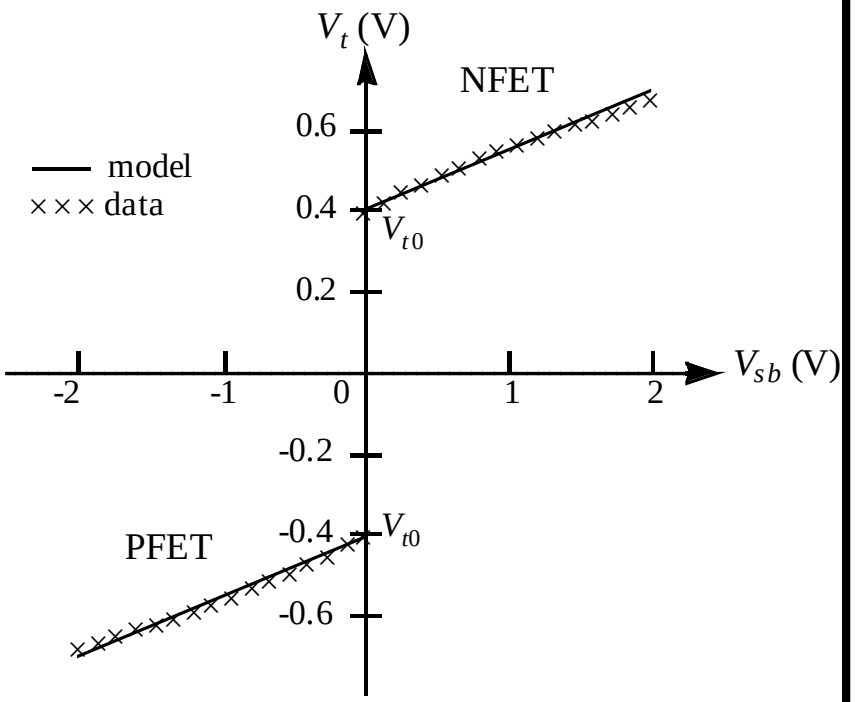
MOSFET V_t and the Body Effect

• ***Body effect***: V_t is a function of V_{sb}. When the source-body junction is reverse-biased, $|V_t|$ increases.

• ***Body effect coefficient***:

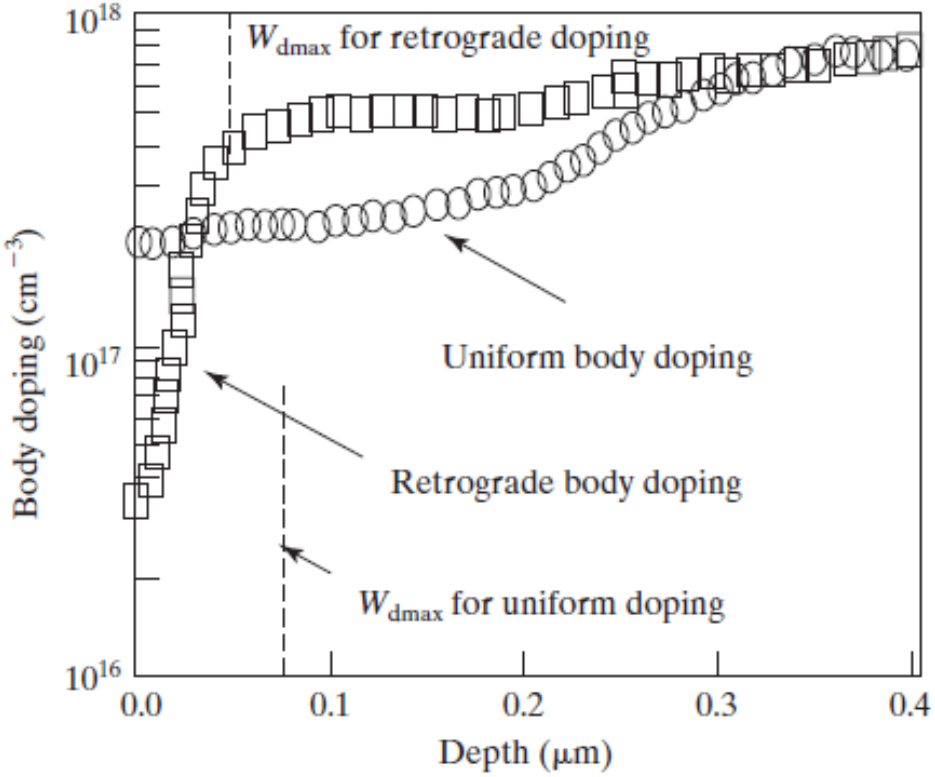
$$V_t = V_{t0} + \alpha V_{sb}$$

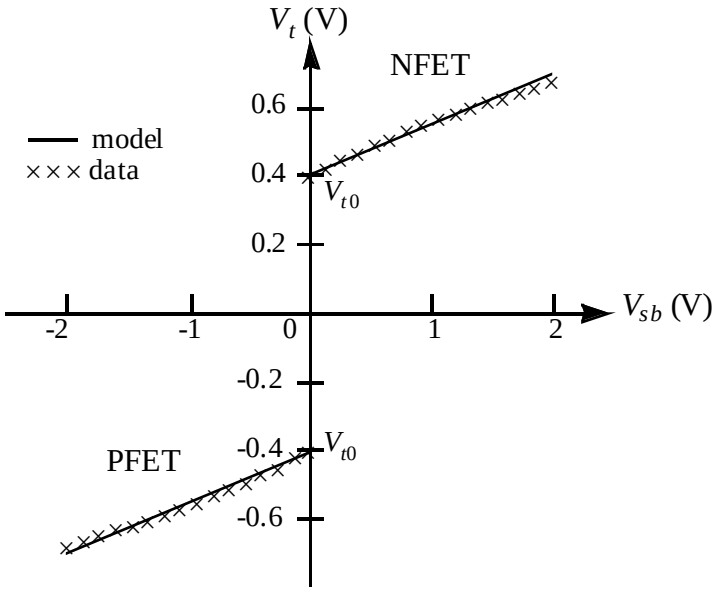
$$\alpha = C_{dep}/C_{oxe}$$
$$= 3T_{oxe} / W_{dep}$$



Body effect slows down circuits? How can it be reduced?

Retrograde Body Doping Profiles





- W_{dep} does not vary with V_{sb}.
- Retrograde doping is popular because it reduces off-state leakage and allows higher surface mobility.

Uniform Body Doping

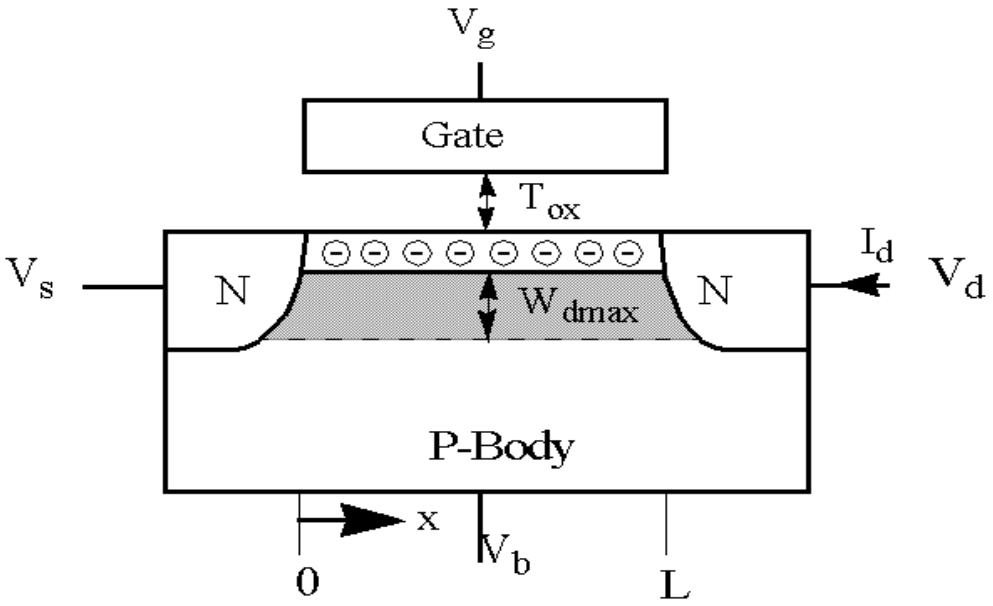
When the source/body junction is reverse-biased, there are two quasi-Fermi levels (E_{fn} and E_{fp}) which are separated by qV_{sb}. An NMOSFET reaches threshold of inversion when E_c is close to E_{fn}, not E_{fp}. This requires the band-bending to be $2\phi_B + V_{sb}$, not $2\phi_B$.

$$V_t = V_{t0} + \frac{\sqrt{qN_a 2\varepsilon_s}}{C_{oxe}}\left(\sqrt{2\phi_B + V_{sb}} - \sqrt{2\phi_B}\right)$$

$$\equiv V_{t0} + \gamma\left(\sqrt{2\phi_B + V_{sb}} - \sqrt{2\phi_B}\right)$$

γ is the ***body-effect parameter***.

6.5 Q_{inv} in MOSFET



- Channel voltage
  $V_c = V_s$ at $x = 0$ and
  $V_c = V_d$ at $x = L$.

- $Q_{inv} = -C_{oxe}(V_{gs} - V_{cs} - V_{t0} - \alpha\,(V_{sb} + V_{cs})$
  $= -C_{oxe}(V_{gs} - V_{cs} - (V_{t0} + \alpha\, V_{sb}) - \alpha\, V_{cs})$
  $= -C_{oxe}(V_{gs} - mV_{cs} - V_t)$

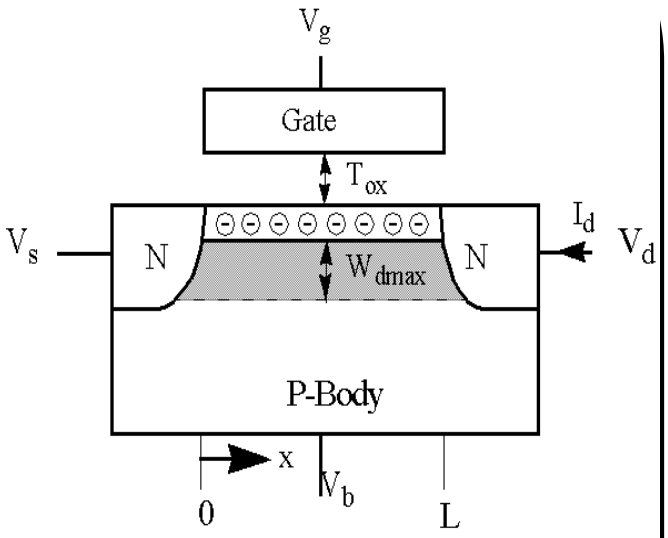
- $m \equiv 1 + \alpha = 1 + 3T_{oxe}/W_{dmax}$
  m is called the ***body-effect factor*** or ***bulk-charge factor***

6.6 Basic MOSFET IV Model

$$I_{ds} = WQ_{inv}v = WQ_{inv}\mu_{ns}\mathbf{E}$$
$$= WC_{oxe}(V_{gs} - mV_{cs} - V_t)\mu_{ns}dV_{cs}/dx$$

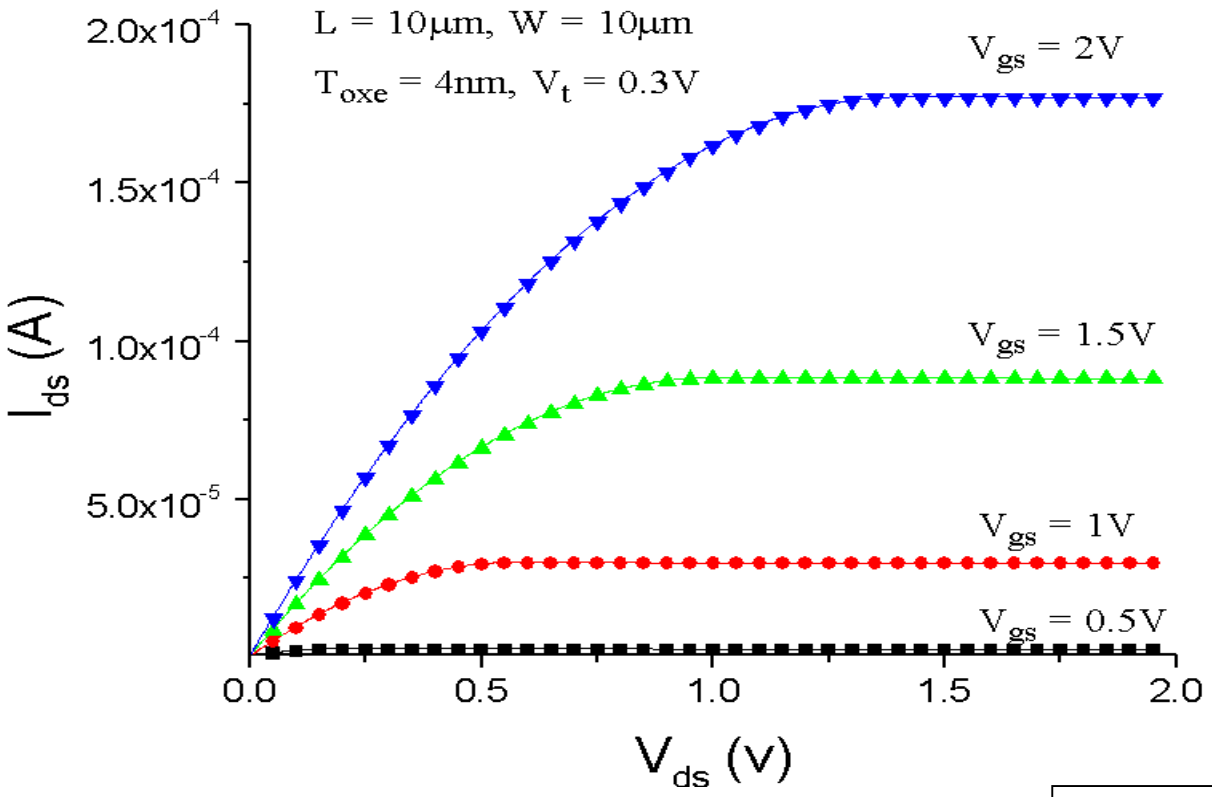
$$\int_0^L I_{ds}dx = WC_{oxe}\mu_{ns}\int_0^{V_{ds}}(V_{gs} - mV_{cs} - V_t)dV_{cs}$$

$$I_{ds}L = WC_{oxe}\mu_{ns}(V_{gs} - V_t - mV_{ds}/2)V_{ds}$$

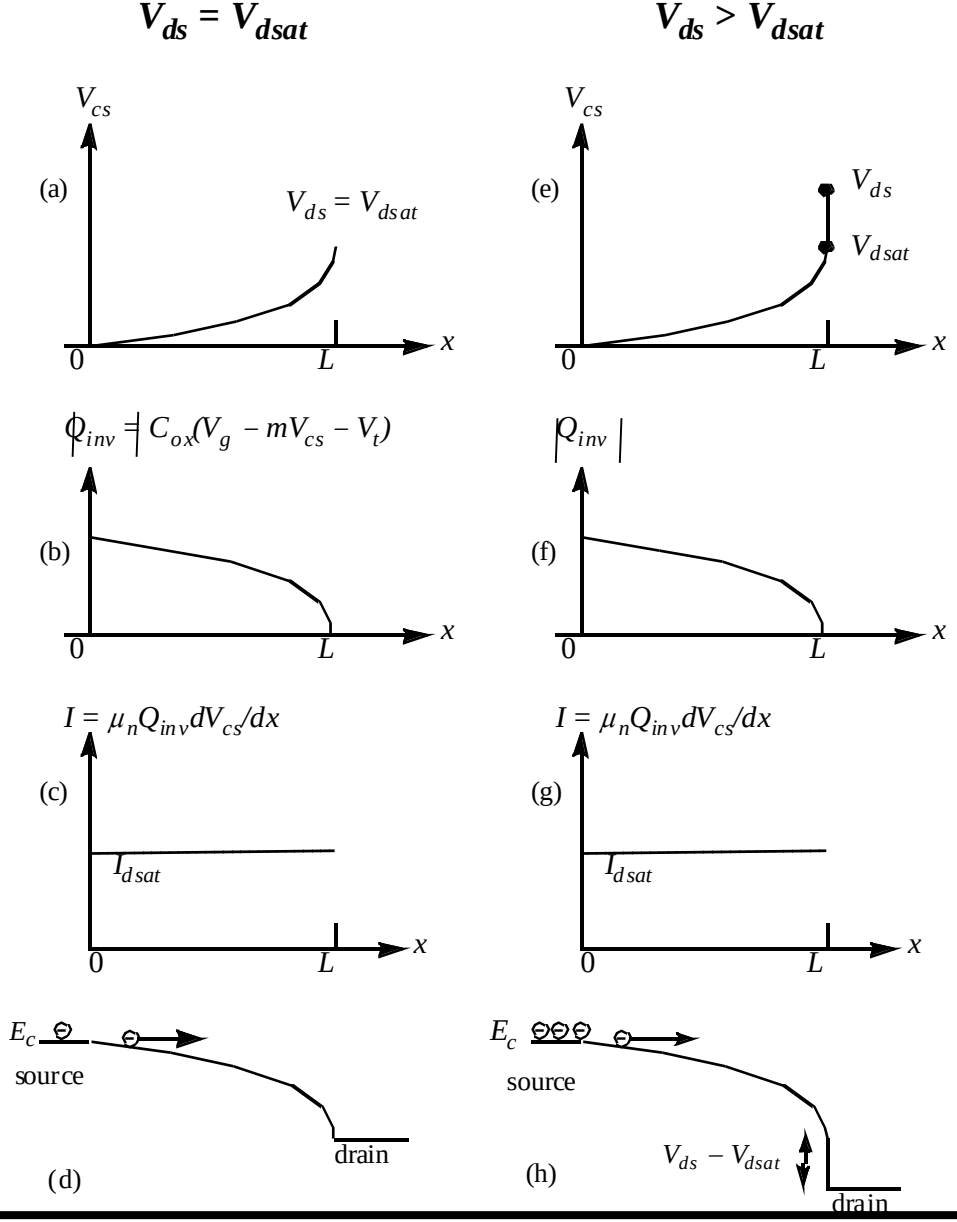


$$I_{ds} = \frac{W}{L}C_{oxe}\mu_s(V_{gs} - V_t - \frac{m}{2}V_{ds})V_{ds}$$

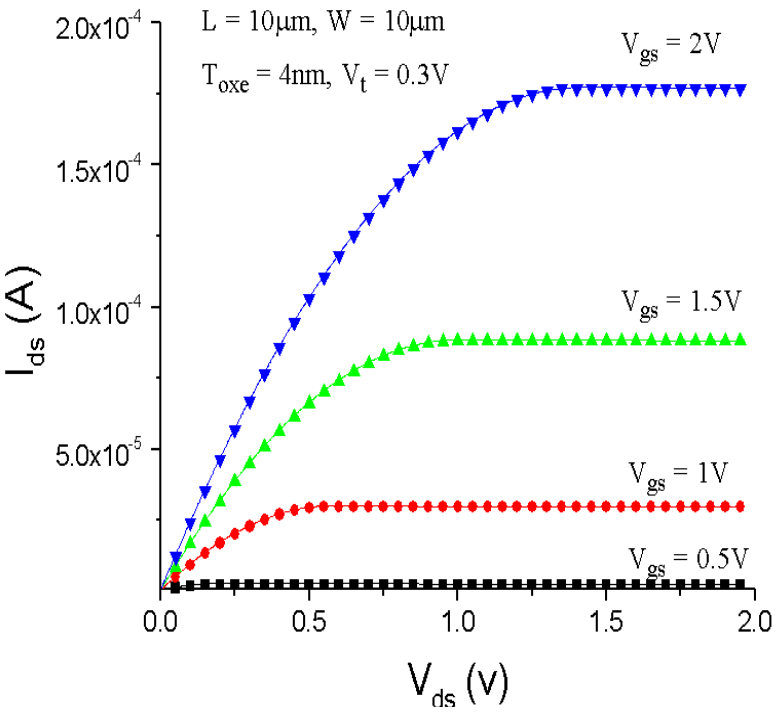
V_{dsat} : Drain Saturation Voltage



$$\frac{dI_{ds}}{dV_{ds}} = 0 = \frac{W}{L} C_{oxe} \mu_{ns} (V_{gs} - V_t - mV_{ds}) \Rightarrow \boxed{V_{dsat} = \frac{V_{gs} - V_t}{m}}$$


$V_{ds} = V_{dsat}$
$V_{ds} > V_{dsat}$
V_{cs}
(a)
$V_{ds} = V_{dsat}$
0
L
x
V_{cs}
(e)
V_{ds}
V_{dsat}
0
L
x
$Q_{inv} = C_{ox}(V_g - mV_{cs} - V_t)$
(b)
0
L
x
Q_{inv}
(f)
0
L
x
$I = \mu_n Q_{inv} dV_{cs}/dx$
(c)
I_{dsat}
0
L
x
$I = \mu_n Q_{inv} dV_{cs}/dx$
(g)
I_{dsat}
0
L
x
E_c
source
drain
(d)
E_c
source
$V_{ds} - V_{dsat}$
drain
(h)

Saturation Current and Transconductance



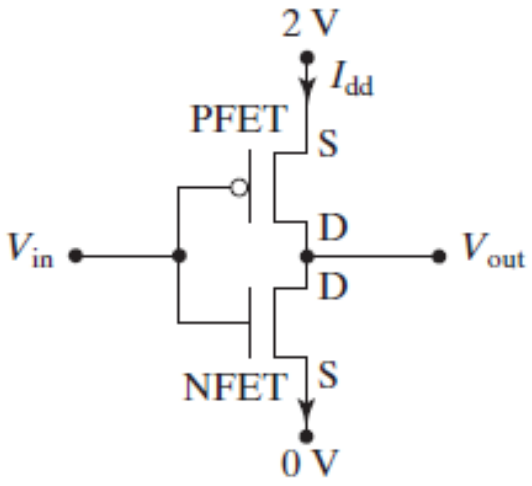
- linear region, saturation region

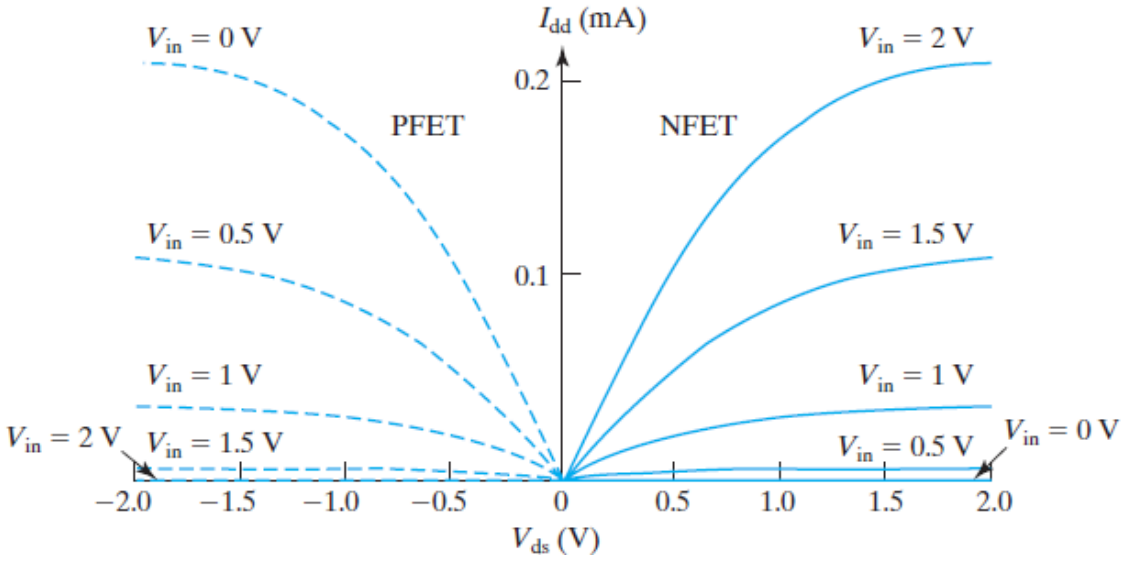
$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_{ns} (V_{gs} - V_t)^2$$

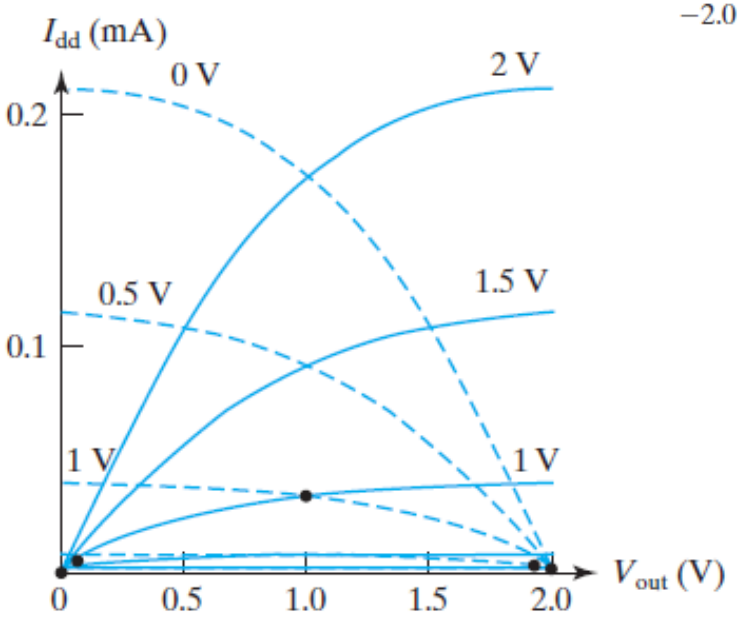
- transconductance: $g_m = dI_{ds}/dV_{gs}$

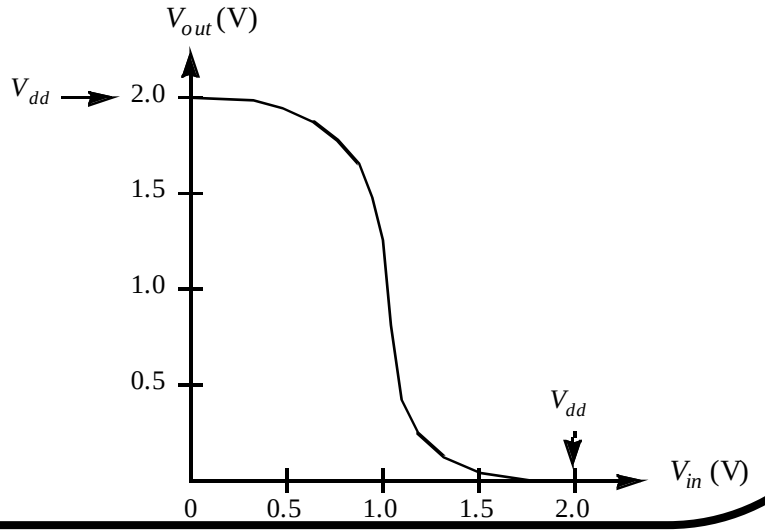
$$g_{msat} = \frac{W}{mL} C_{oxe} \mu_{ns} (V_{gs} - V_t)$$

6.7.1 CMOS Inverter--voltage transfer curve

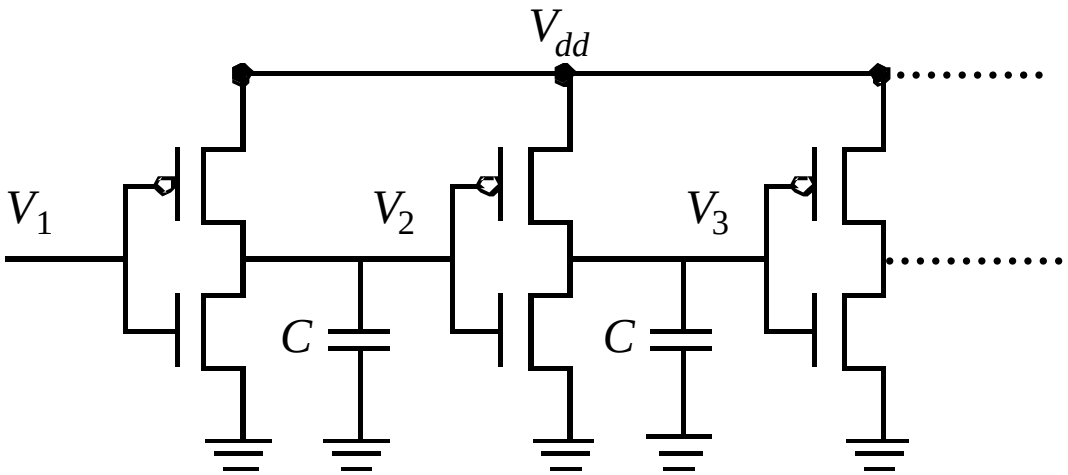


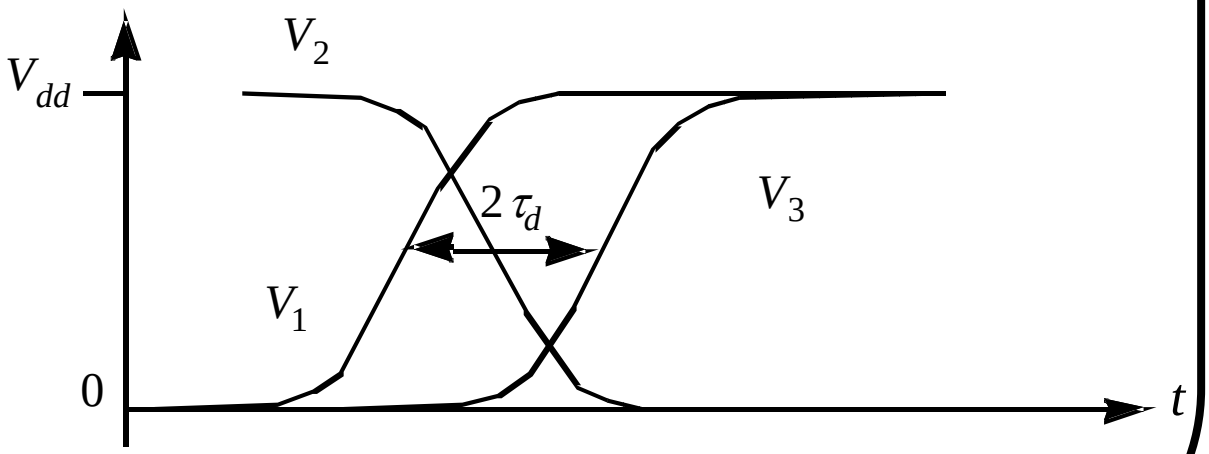






6.7.2 Inverter Speed – propagation delay





τ_d : propagation delay

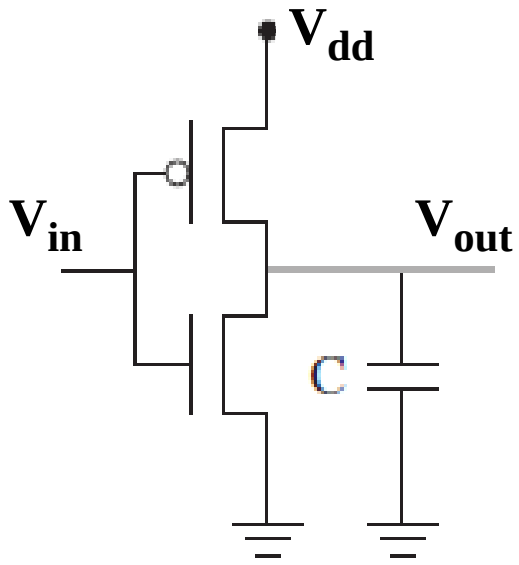
6.7.2 Inverter Speed - Impact of I_{on}

$$\tau_d \equiv \frac{1}{2}(pull-down\ delay\ +\ pull-up\ delay)$$

$$pull-up\ delay \approx \frac{CV_{dd}}{2I_{onP}}$$

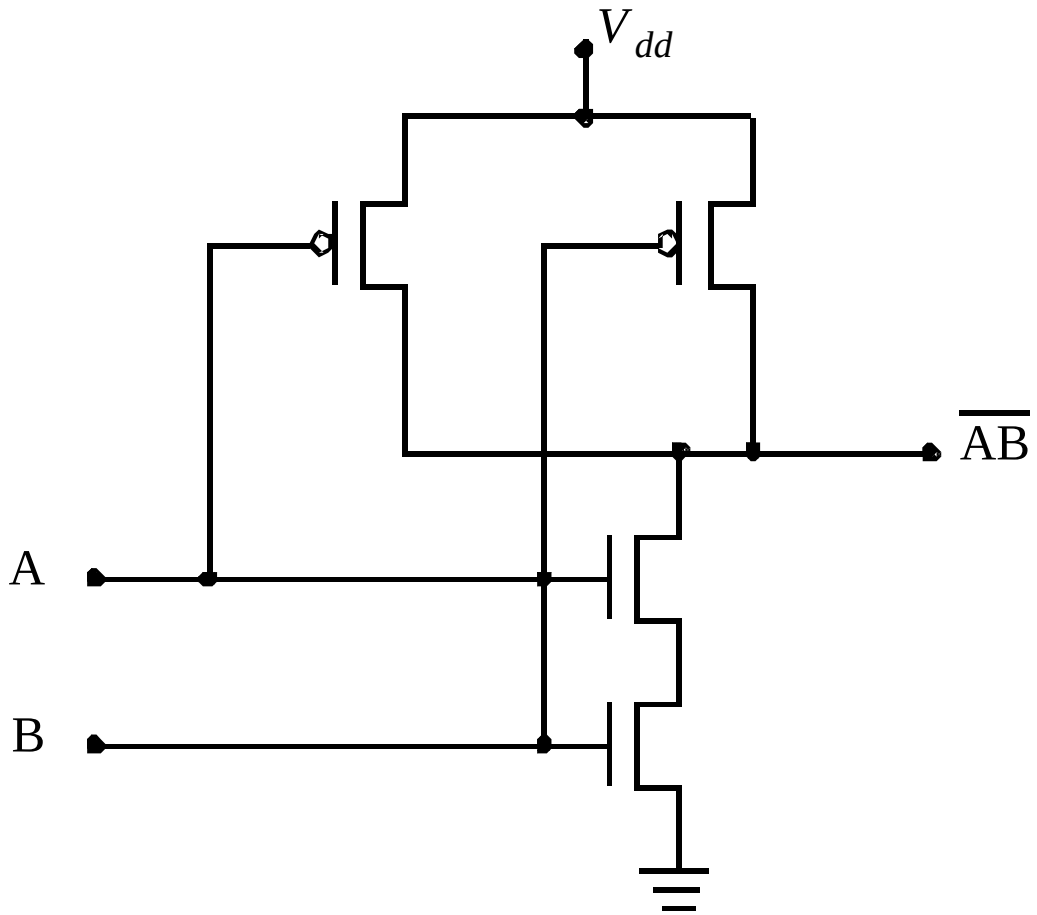
$$pull-down\ delay \approx \frac{CV_{dd}}{2I_{onN}}$$

$$\tau_d = \frac{CV_{dd}}{4}\left(\frac{1}{I_{onN}} + \frac{1}{I_{onP}}\right)$$



How can the speed of an inverter circuit be improved?

Logic Gates



This two-input NAND gate and many other logic gates are extensions of the inverter.

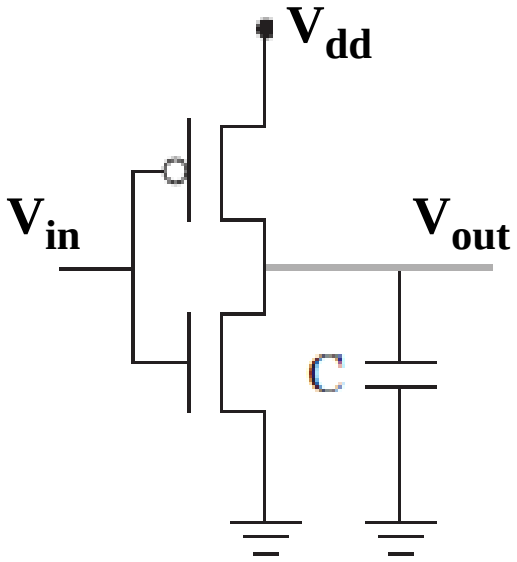
6.7.3 Power Consumption

$$P_{dynamic} = V_{dd} \times average\ current = k\,CV_{dd}^2\,f$$

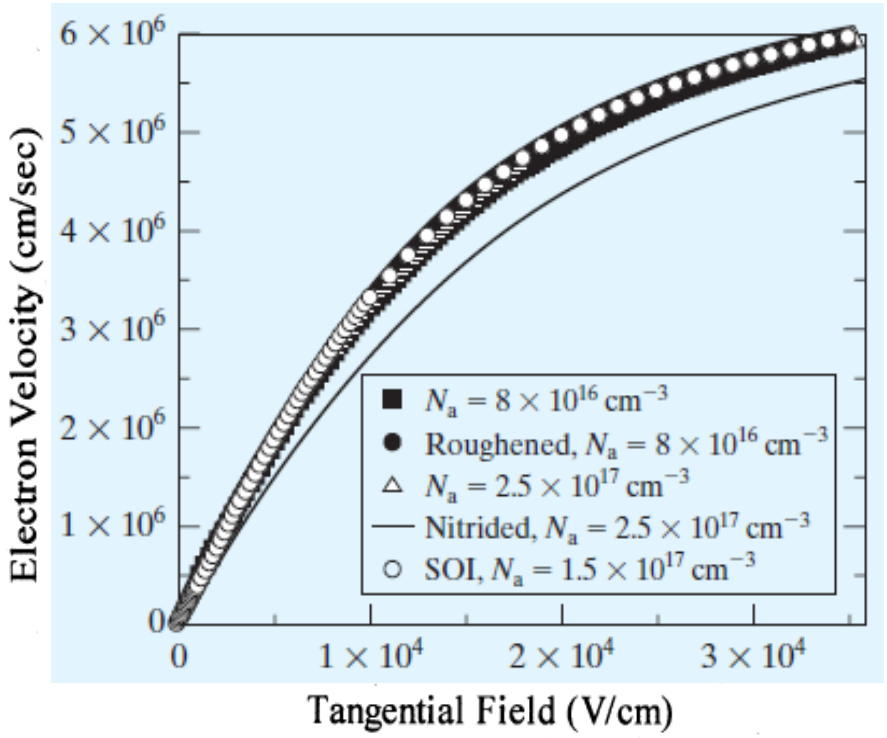
$$P_{static} = V_{dd} I_{off}$$

Total power consumption

$$P = P_{dynamic} + P_{static}$$



6.8 Velocity Saturation



$$v = \frac{\mu_{ns}\mathcal{E}}{1 + \dfrac{\mathcal{E}}{\mathcal{E}_{sat}}}$$

$$\mathcal{E} << \mathcal{E}_{sat} : v = \mu_{ns}\mathcal{E}$$

$$\mathcal{E} >> \mathcal{E}_{sat} : v = \mu_{ns}\mathcal{E}_{sat}$$

- Velocity saturation has large and deleterious effect on the I_{on} of MOSFETS

6.9 MOSFET IV Model with Velocity Saturation

$$I_{ds} = WQ_{inv}v$$

$$I_{ds} = WC_{oxe}(V_{gs} - mV_{cs} - V_t)\frac{\mu_{ns}dV_{cs}/dx}{1+\frac{dV_{cs}}{dx}/\mathcal{E}_{sat}}$$

$$\int_0^L I_{ds}dx = \int_0^{V_{ds}} [WC_{oxe}\mu_{ns}(V_{gs} - mV_{cs} - V_t) - I_{ds}/\mathcal{E}_{sat}]dV_{cs}$$

$$I_{ds}L = WC_{oxe}\mu_{ns}(V_{gs} - V_t - \frac{m}{2}V_{ds})V_{ds} - I_{ds}V_{ds}/\mathcal{E}_{sat}$$

6.9 MOSFET IV Model with Velocity Saturation

$$I_{ds} = \frac{\frac{W}{L} C_{oxe} \mu_{ns} \left(V_{gs} - V_t - \frac{m}{2} V_{ds}\right) V_{ds}}{1 + \frac{V_{ds}}{\mathcal{E}_{sat} L}}$$

$$\boxed{I_{ds} = \frac{long\text{-}channel\ I_{ds}}{1 + V_{ds} / \mathcal{E}_{sat} L}}$$

6.9 MOSFET IV Model with Velocity Saturation

Solving $\frac{dI_{ds}}{dV_{ds}} = 0,$

$$V_{dsat} = \frac{2(V_{gs} - V_t)/m}{1 + \sqrt{1 + 2(V_{gs} - V_t)/m\mathcal{E}_{sat}L}}$$

A simpler and more accurate V_{dsat} is:

$$\boxed{\frac{1}{V_{dsat}} = \frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat}L}}$$

$$\mathcal{E}_{sat} \equiv \frac{2v_{sat}}{\mu_{ns}}$$

EXAMPLE: Drain Saturation Voltage

Question: *At V_{gs} = 1.8 V, what is the V_{dsat} of an NFET with T_{oxe} = 3 nm, V_t = 0.25 V, and W_{dmax} = 45 nm for (a) L =10 μm, (b) L = 1 um, (c) L = 0.1 μm, and (d) L = 0.05 μm?*

Solution: *From V_{gs}, V_t, and T_{oxe}, μ_{ns} is 200 $cm^2V^{-1}s^{-1}$.*

$$\mathcal{E}_{sat} = 2v_{sat}/\mu_{ns} = 8 \times 10^4 \text{ V/cm}$$

$$m = 1 + 3T_{oxe}/W_{dmax} = 1.2$$

$$V_{dsat} = \left(\frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat} L} \right)^{-1}$$

EXAMPLE: Drain Saturation Voltage

$$V_{dsat} = \left(\frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat} L} \right)^{-1}$$

(a) $L = 10\ \mu m$, $V_{dsat} = (1/1.3\text{V} + 1/80\text{V})^{-1} = 1.3$ V

(b) $L = 1\ \mu m$, $V_{dsat} = (1/1.3\text{V} + 1/8\text{V})^{-1} = 1.1$ V

(c) $L = 0.1\ \mu m$, $V_{dsat} = (1/1.3\text{V} + 1/.8\text{V})^{-1} = 0.5$ V

(d) $L = 0.05\ \mu m$, $V_{dsat} = (1/1.3\text{V} + 1/.4\text{V})^{-1} = 0.3$ V

I_{dsat} with Velocity Saturation

Substituting V_{dsat} for V_{ds} in I_{ds} equation gives:

$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_s \frac{(V_{gs} - V_t)^2}{1 + \frac{V_{gs} - V_t}{m\mathcal{E}_{sat} L}} = \frac{long\text{-}channel\ I_{dsat}}{1 + \frac{V_{gs} - V_t}{m\mathcal{E}_{sat} L}}$$

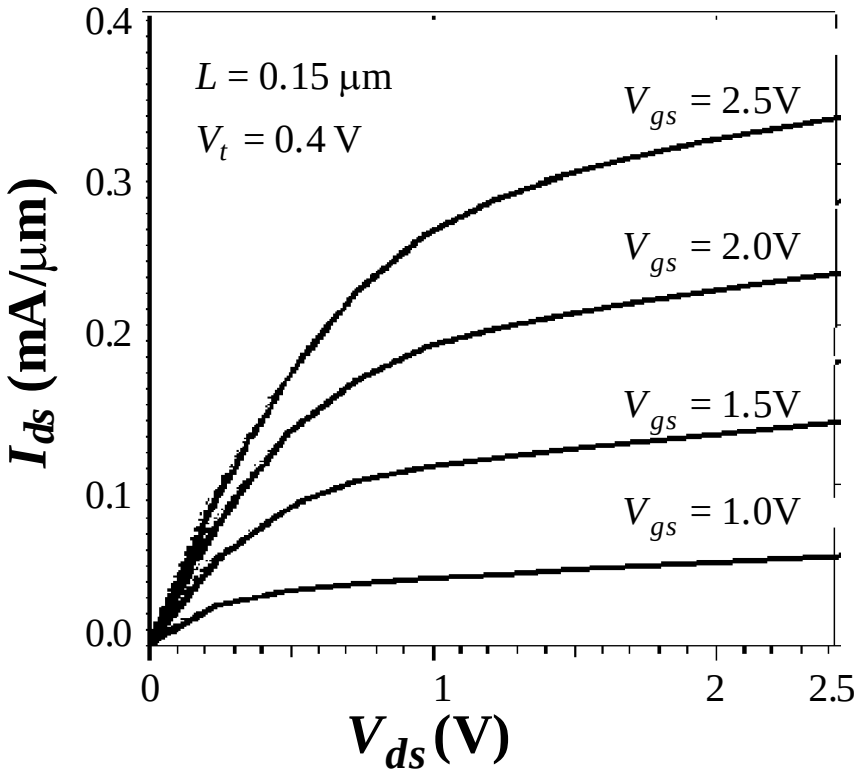
Very short channel case: $\mathcal{E}_{sat} L << V_{gs} - V_t$

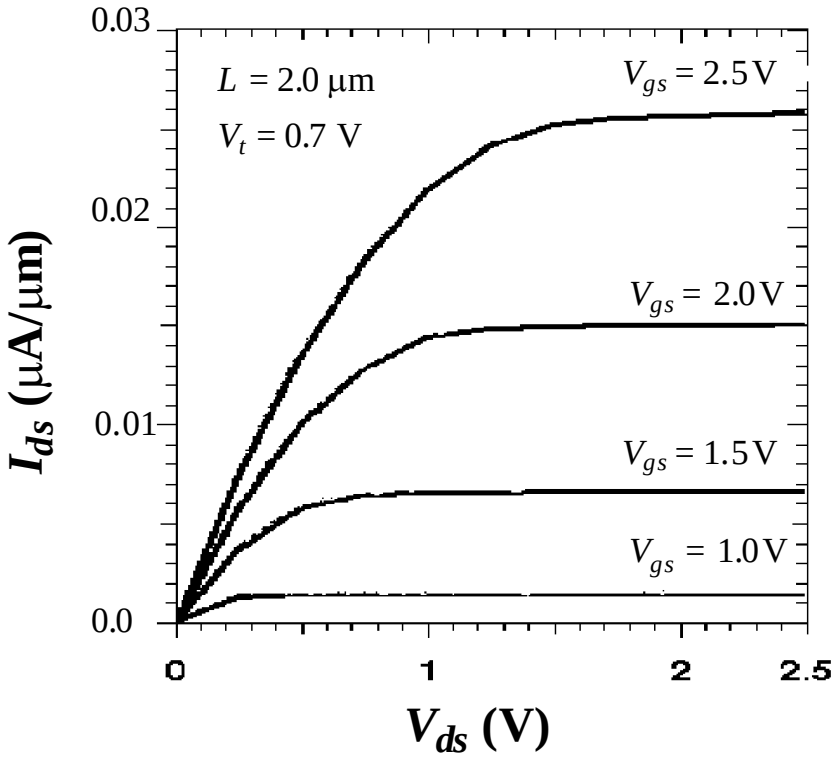
$$I_{dsat} = W v_{sat} C_{oxe} (V_{gs} - V_t - m\mathcal{E}_{sat} L)$$

$$I_{dsat} = W v_{sat} C_{oxe} (V_{gs} - V_t)$$

- I_{dsat} is proportional to V_{gs}–V_t rather than $(V_{gs} - V_t)^2$, not as sensitive to L as $1/L$.

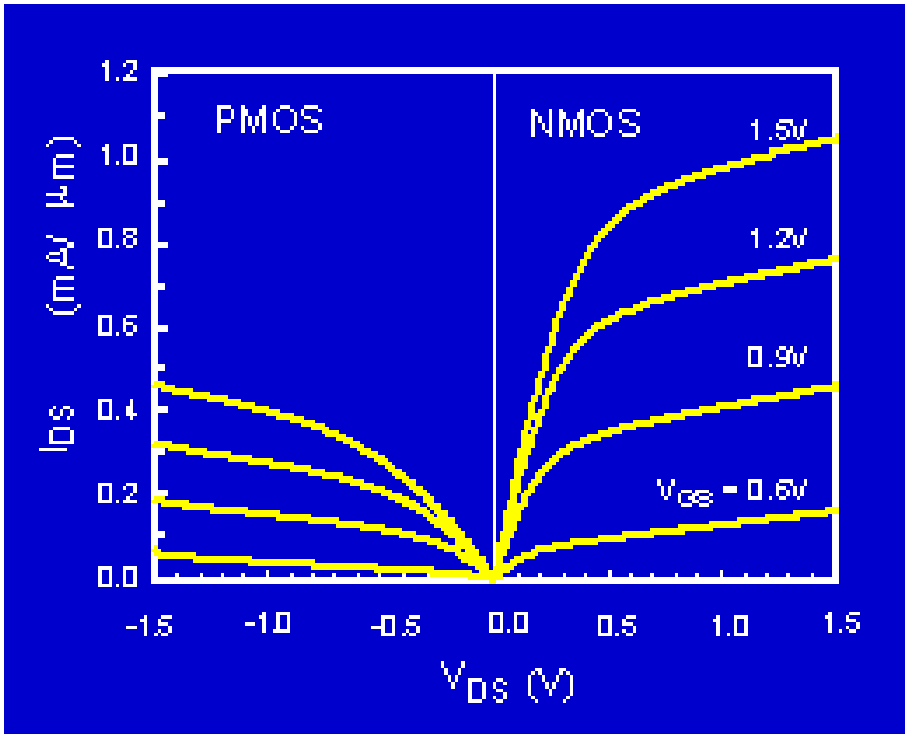
Measured MOSFET IV





What is the main difference between the V_g dependence of the long- and short-channel length IV curves?

PMOS and NMOS IV Characteristics



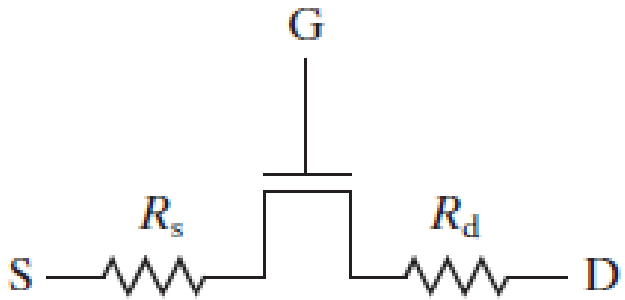
The PMOS IV is qualitatively similar to the NMOS IV, but the current is about half as large. How can we design a CMOS inverter so that its voltage transfer curve is symmetric?

6.9.1 Velocity Saturation vs. Pinch-Off

Current saturation : the carrier velocity reaches V_{sat} at the drain.

Instead of the **pinch-off region**, there is a **velocity saturation region** next to the drain where Q_{inv} is a constant (I_{dsat}/W_{vsat}).

6.10 Parasitic Source-Drain Resistance

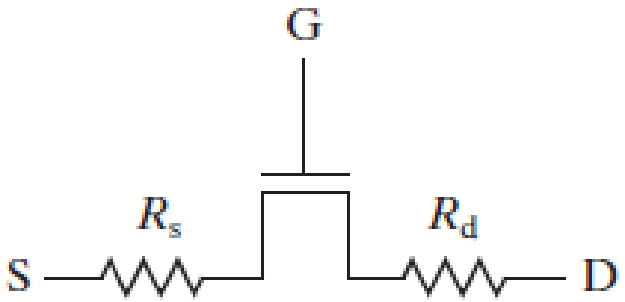


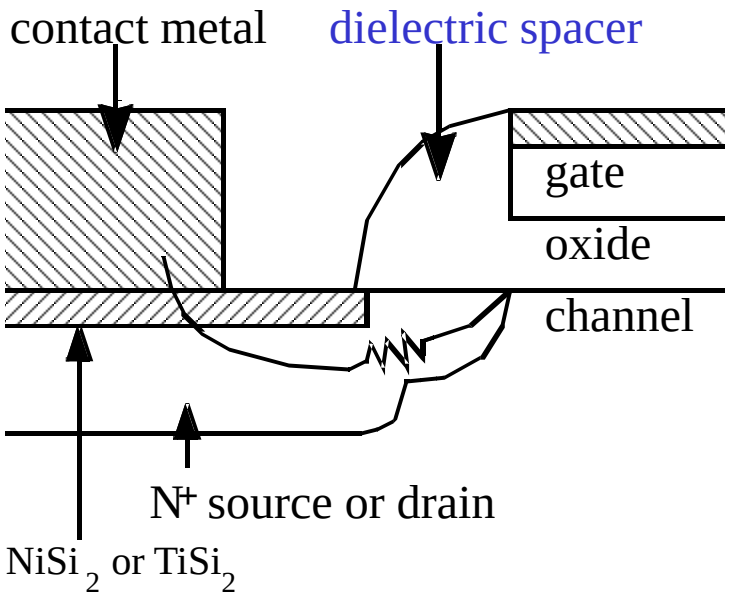
- If $I_{dsat0} \propto V_g - V_t$, $I_{dsat} = \dfrac{I_{dsat0}}{1 + \dfrac{I_{dsat0} R_s}{(V_{gs} - V_t)}}$

- I_{dsat} can be reduced by about 15% in a 0.1μm MOSFET. Effect is greater in shorter MOSFETs.

- $V_{dsat} = V_{dsat0} + I_{dsat}(R_s + R_d)$

SALICIDE (Self-Aligned Silicide) Source/Drain



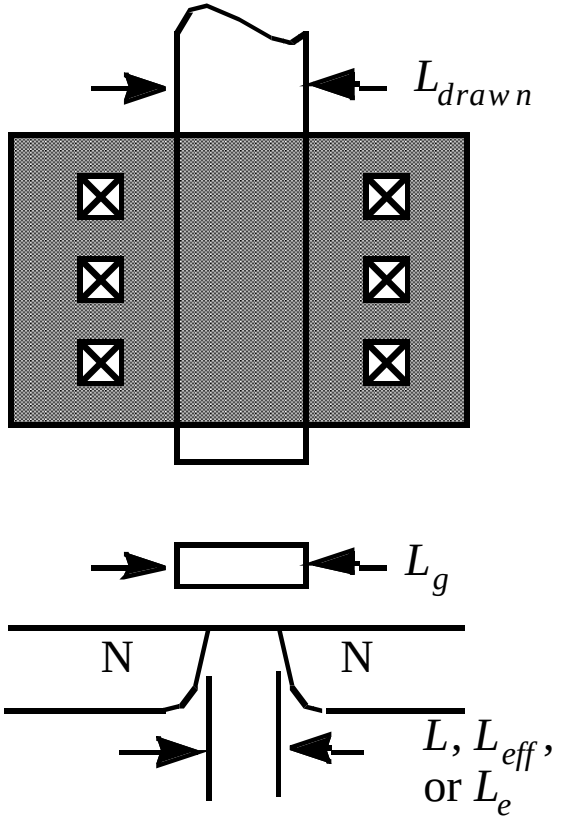


After the spacer is formed, a Ti or Mo film is deposited. Annealing causes the silicide to be formed over the source, drain, and gate. Unreacted metal (over the spacer) is removed by wet etching.

Question:

- What is the purpose of siliciding the source/drain/gate?
- What is self-aligned to what?

Definitions of Channel Length



$$L \equiv L_g - \Delta L$$

6.11 Extraction of the Series Resistance and the Effective Channel Length

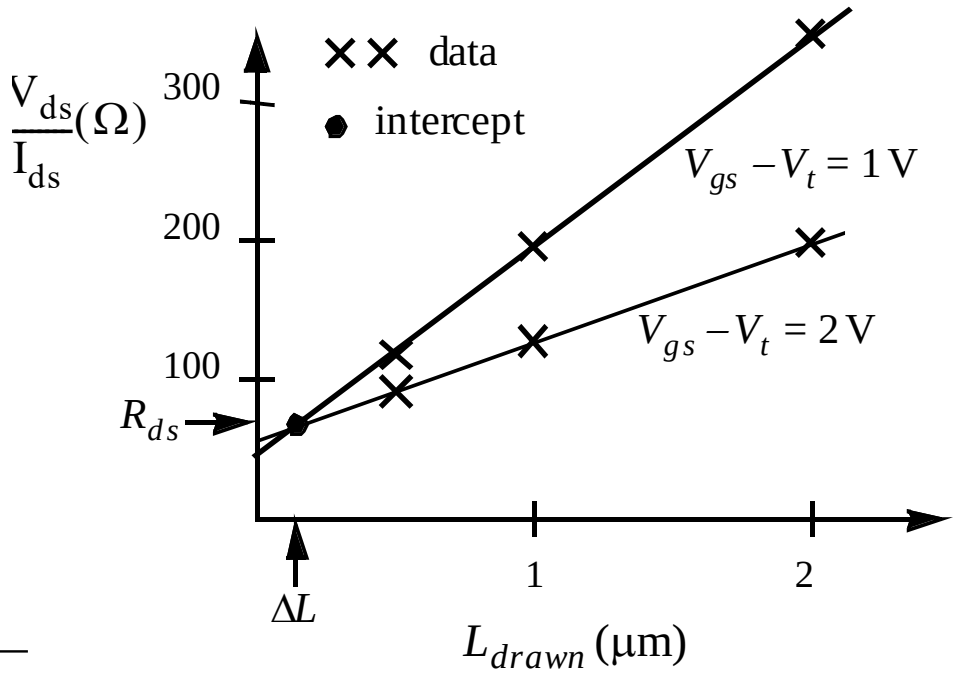
$$I_{ds} = \frac{WC_{oxe}\mu_s V_{ds}}{L_{drawn} - \Delta L}(V_{gs} - V_t)$$

$$V_{ds} = \frac{I_{ds}(L_{drawn} - \Delta L)}{WC_{oxe}(V_{gs} - V_t)\mu_s}$$

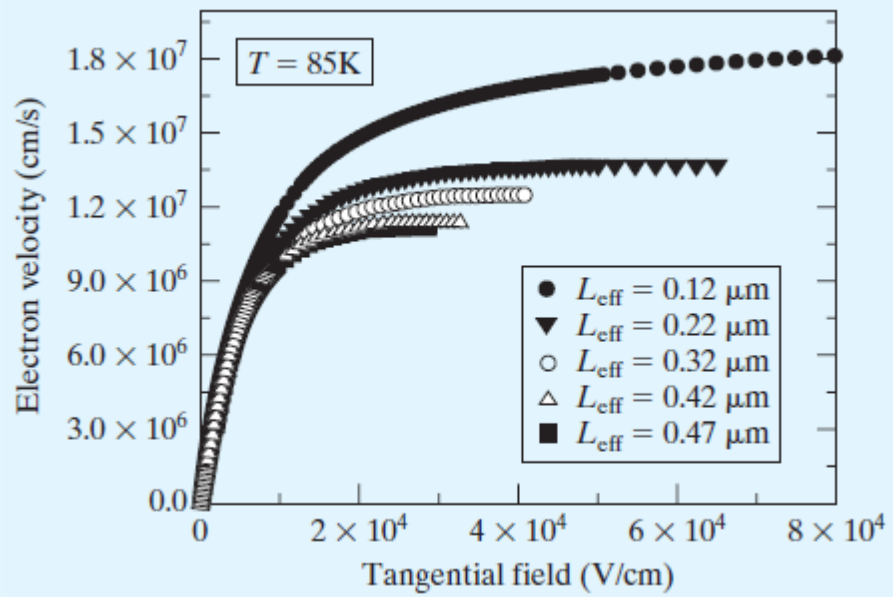
Include series resistance,

$R_{ds} \equiv R_d + R_s$,

$$\frac{V_{ds}}{I_{ds}} = R_{ds} + \frac{L_{drawn} - \Delta L}{WC_{oxe}(V_{gs} - V_t)\mu_s}$$

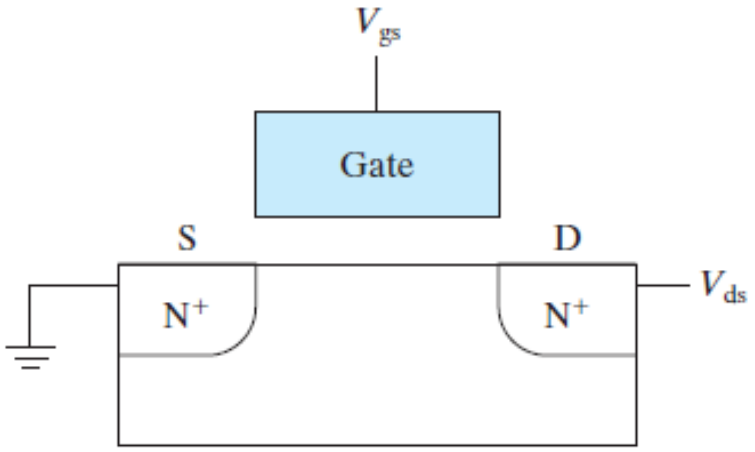


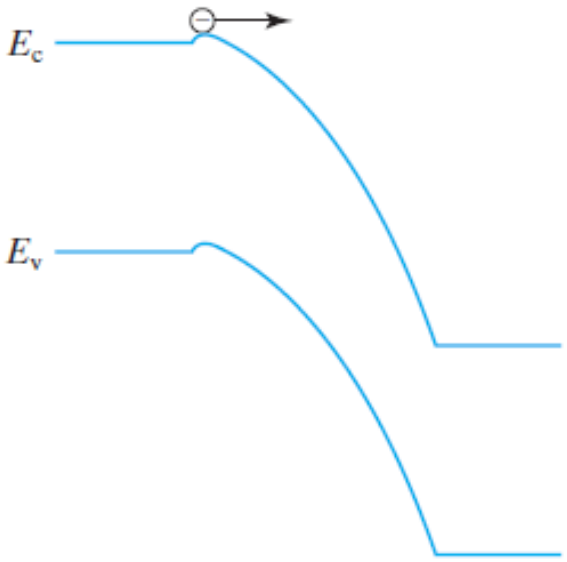
6.12 Velocity Overshoot



- Velocity saturation should not occur in very short MOSFETs.
- This velocity overshoot could lift the limit on Ids .
- *But…*

6.12 Source Velocity Limit





- Carrier velocity is limited by the thermal velocity with which they enter the channel from the source.

- $I_{dsat} = WBv_{thx}Q_{inv}$
  $= WBv_{thx}C_{oxe}(V_{gs} - V_t)$

- Similar to

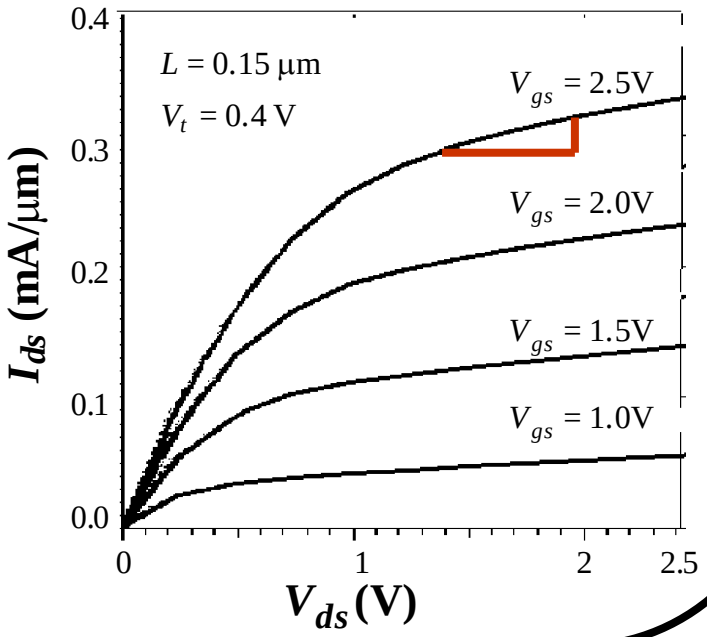
$$I_{dsat} = Wv_{sat}C_{oxe}(V_{gs} - V_t)$$

6.13 Output Conductance

- I_{dsat} does NOT saturate in the saturation region, especially in short channel devices!
- The slope of the I_{ds}-V_{ds} curve in the saturation region is called the **output conductance (g_{ds})**,

$$g_{ds} \equiv \frac{dI_{dsat}}{dV_{ds}}$$

- A smaller g_{ds} is desirable for a large voltage gain, which is beneficial to analog and digital circuit applications.



Example of an Amplifier

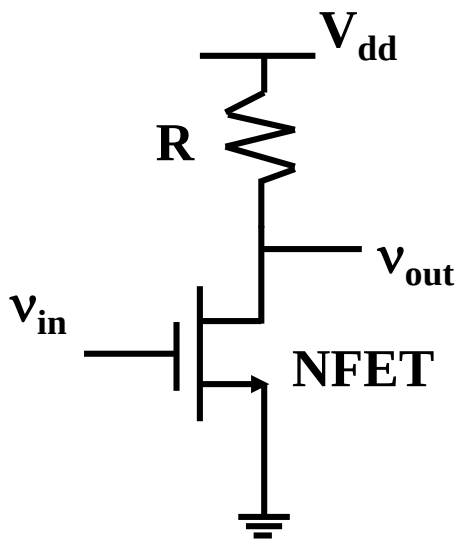
- The transistor operates in the saturation region. A ***small signal*** input, v_{in}, is applied.

$$i_{ds} = g_{msat} \cdot v_{gs} + g_{ds} \cdot v_{ds}$$

$$= g_{msat} \cdot v_{in} + g_{ds} \cdot v_{out}$$

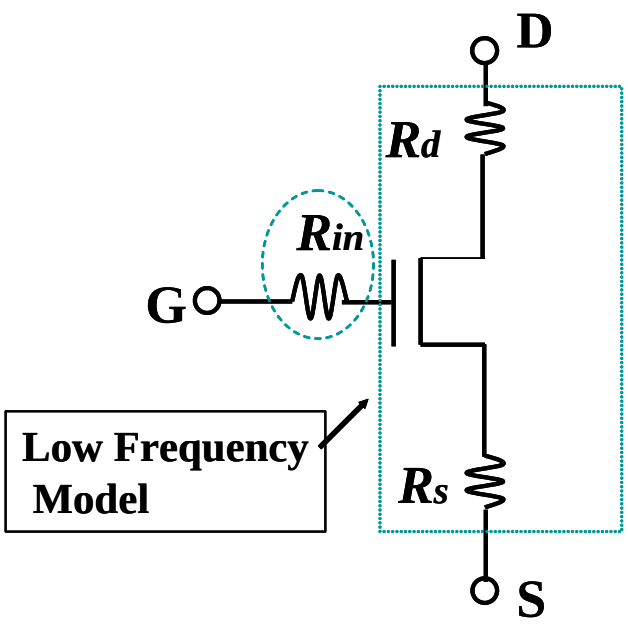
$$i_{ds} = -v_{out} / R \cdot$$

$$\Rightarrow \quad v_{out} = \frac{-g_{msat}}{(g_{ds} + 1/R)} \times v_{in}$$



- The voltage gain is $g_{msat}/(g_{ds} + 1/R)$.
- A smaller g_{ds} is desirable for large voltage gain.
- Maximum available gain (or intrinsic voltage gain) is g_{msat}/g_{ds}

6.14 High-Frequency Performance



High-frequency performance is limited by input R and/or C.

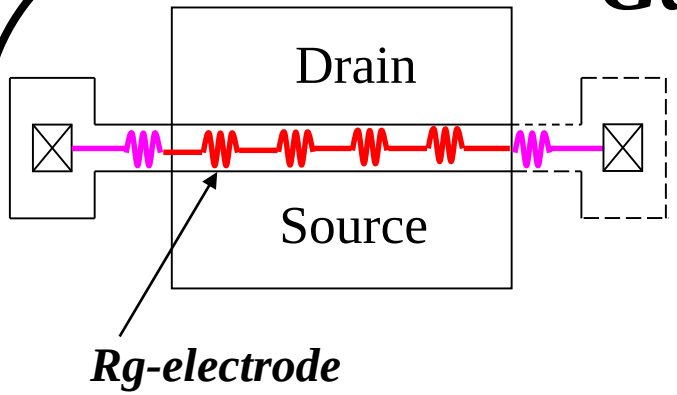
Cutoff frequency (f_T) : Frequency at which the output current becomes equal to the input current.

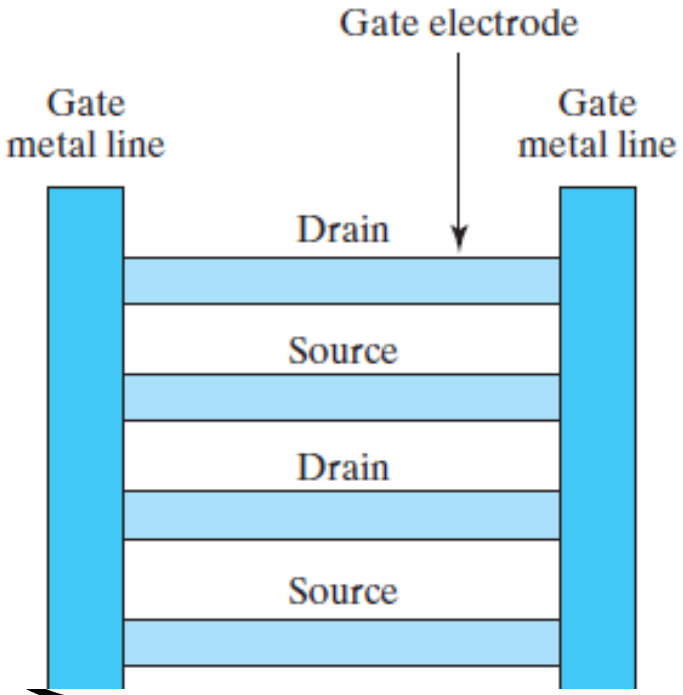
Maximum oscillation frequency (f_{max}) : Frequency at which the power gain drops to unity

$$R_{in} = R_{g-electrode} + R_{ii}$$

Gate-electrode resistance **Intrinsic input resistance**

Gate-Electrode Resistance



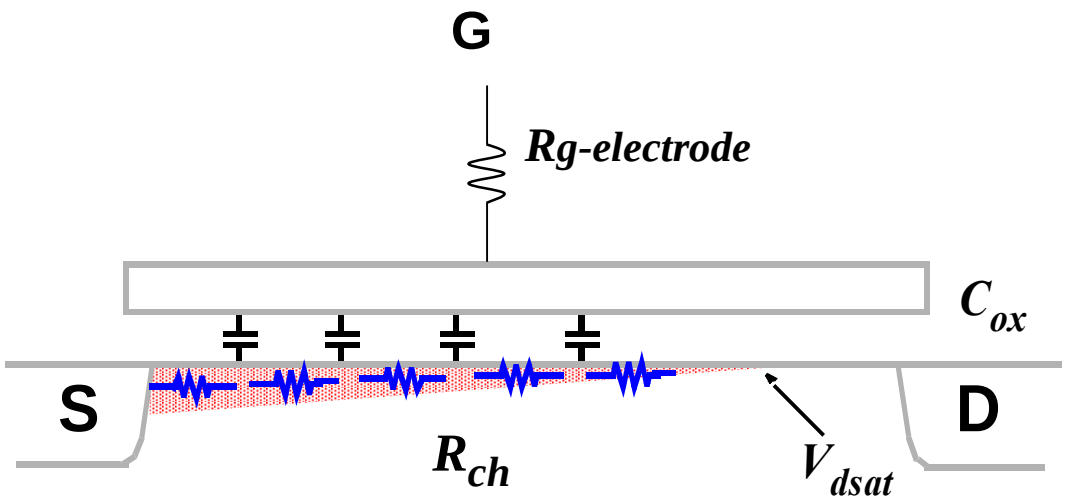


Multi-finger layout greatly reduces the gate electrode resistance

$$R_{g-electrode} = \rho W / 12 T_g L_g N_f^2$$

ρ : resistivity of gate material,
W_f : width of each gate finger,
T_g : gate thickness,
L_g : gate length,
N_f : number of fingers.

Intrinsic Input Resistance



$$R_{ii} = \kappa \int dR_{ch} = \kappa \frac{V_{ds}}{I_{ds}}$$

The gate capacitor current flows through R_{ch} to the source and ground.

6.15 MOSFET Noises

Noise : All that corrupts the signal

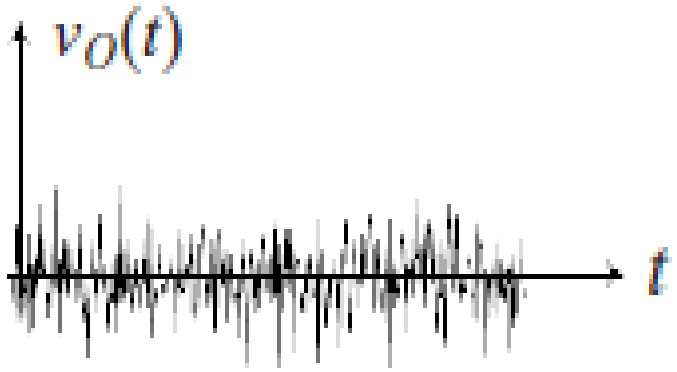
External noise:

- Inductive and capacitive interferences and cross talks created by wiring
- Needs to be controlled with shielding and circuit layout carefully

Fundamental noise:

- Noise inherent to the electronic devices.
- Due to the random behaviors of the electric carriers inside the device

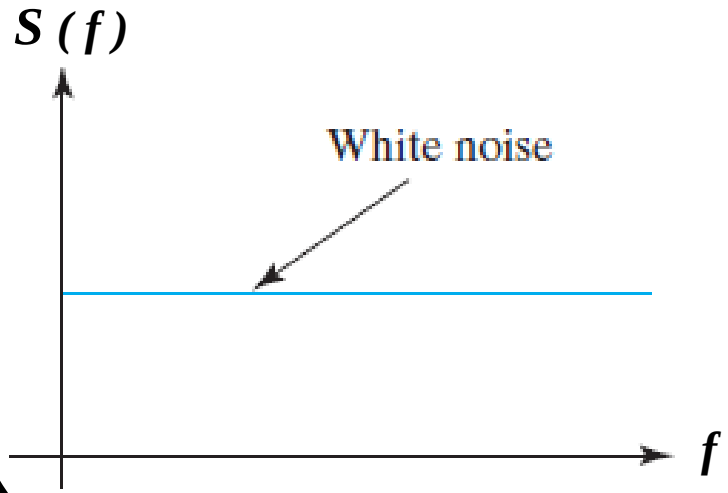
6.15.1 Thermal Noise of a Resistor



Thermal noise: caused by random thermal motion of the charge carriers

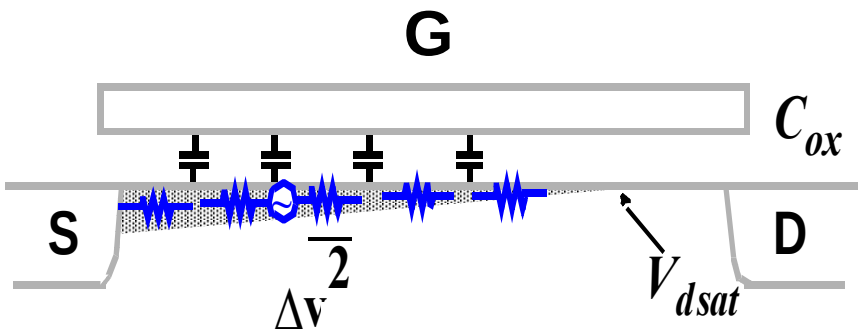
$$\overline{v_n^2} = 4kT\Delta f R = S_{v_n}\Delta f$$

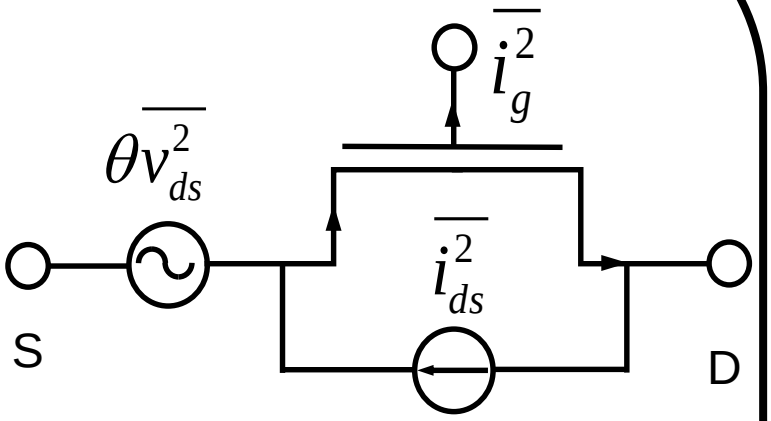
$$\overline{i_n^2} = 4kT\Delta f / R = S_{i_n}\Delta f$$



S **:** noise power density spectrum

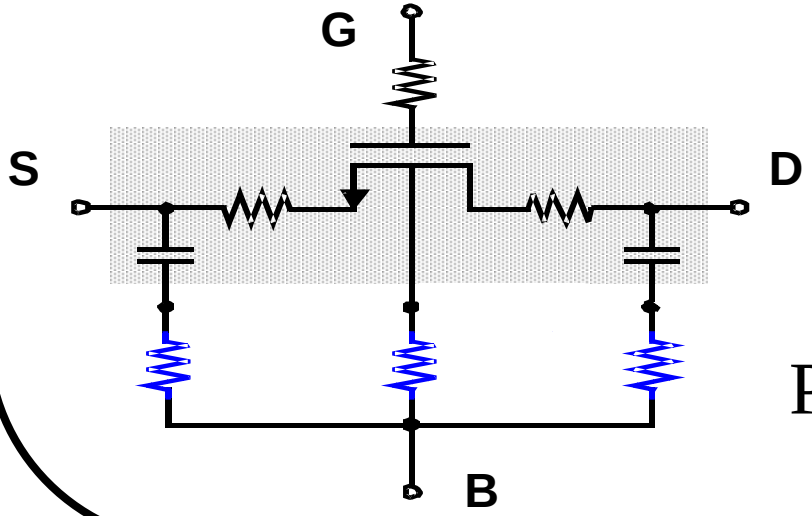
6.15.2 MOSFET Thermal Noise





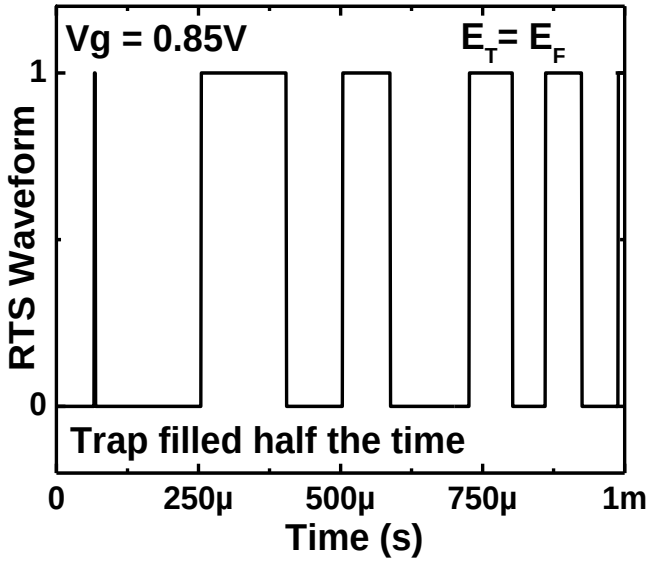
$$\overline{v_{ds}^2} = 4\gamma kT\Delta f / g_{ds}$$

$$\overline{i_{ds}^2} = 4\gamma kT\Delta f g_{ds}$$



Parasitic-resistance noise

6.15.3 MOSFET Flicker Noise

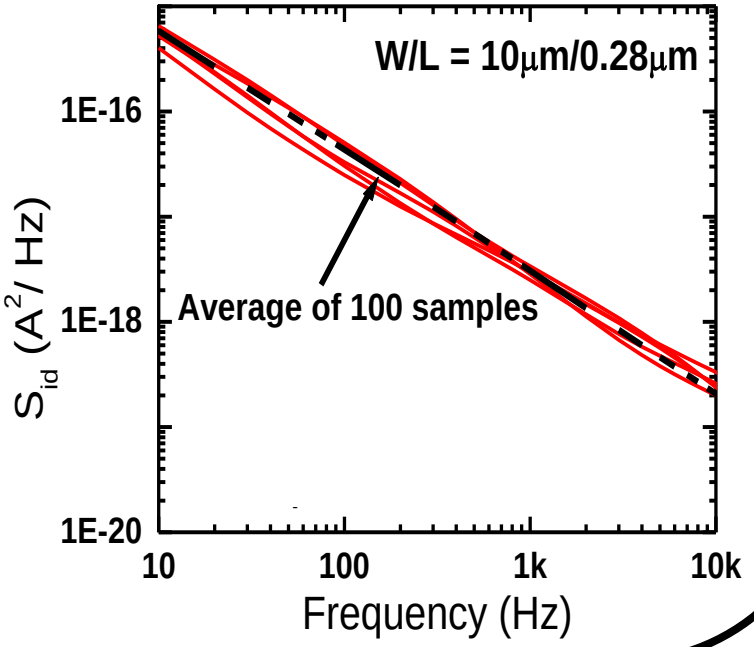


Charge trapping and releasing by a single oxide trap generate Random Telegraph Noise

Many traps produce a 1/f power density spectrum.

1/f noise

$$\overline{i_{ds}^2} = \frac{KF \cdot W}{fL^2 C_{ox}} \left(\frac{I_{ds}}{W}\right)^{AF} \cdot kT\Delta f$$



6.15.4 Signal to Noise Ratio, Noise Factor, Noise Figure

SNR: Signal power ÷ noise power.

Decibel or dB:10 times the base-10 logarithm of the noise power.

$$10 \times \log \frac{S}{N}$$

Noise factor: The ratio of the input SNR and output SNR.

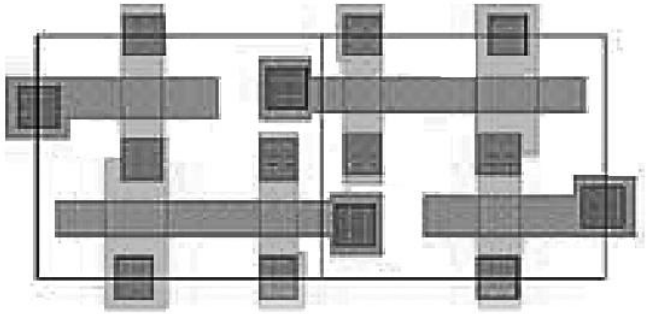
$$F = \frac{S_i / N_i}{S_0 / N_0}$$

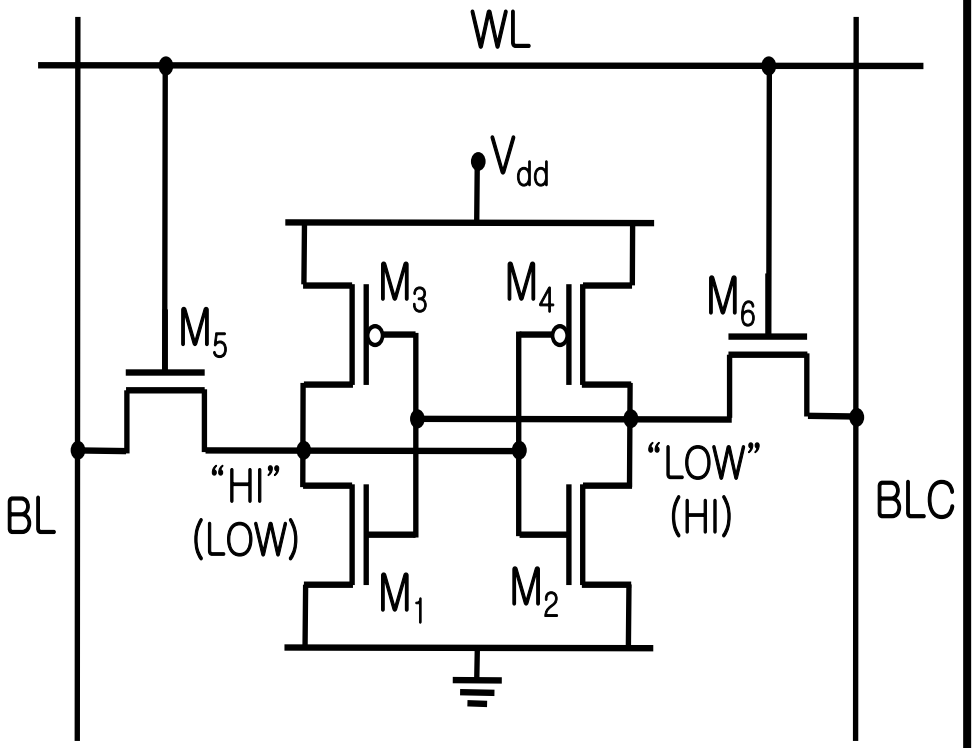
6.16 Memory Devices

	Keep data without power?	*Cell size and cost/bit*	*Rewrite cycles*	*Write-one-byte speed*	*Compatible with basic CMOS fabrication*	*Main applications*
SRAM	*No*	*Large*	*Unlimited*	*Fastest*	*Totally*	*Embedded in logic chips*
DRAM	*No*	*Small*	*Unlimited*	*Fast*	*Needs modification*	*Stand-alone main memory*
Flash memory (NVM)	*Yes*	*Smallest*	*Limited*	*Slow*	*Needs extensive modification*	*Nonvolatile data and code storage*

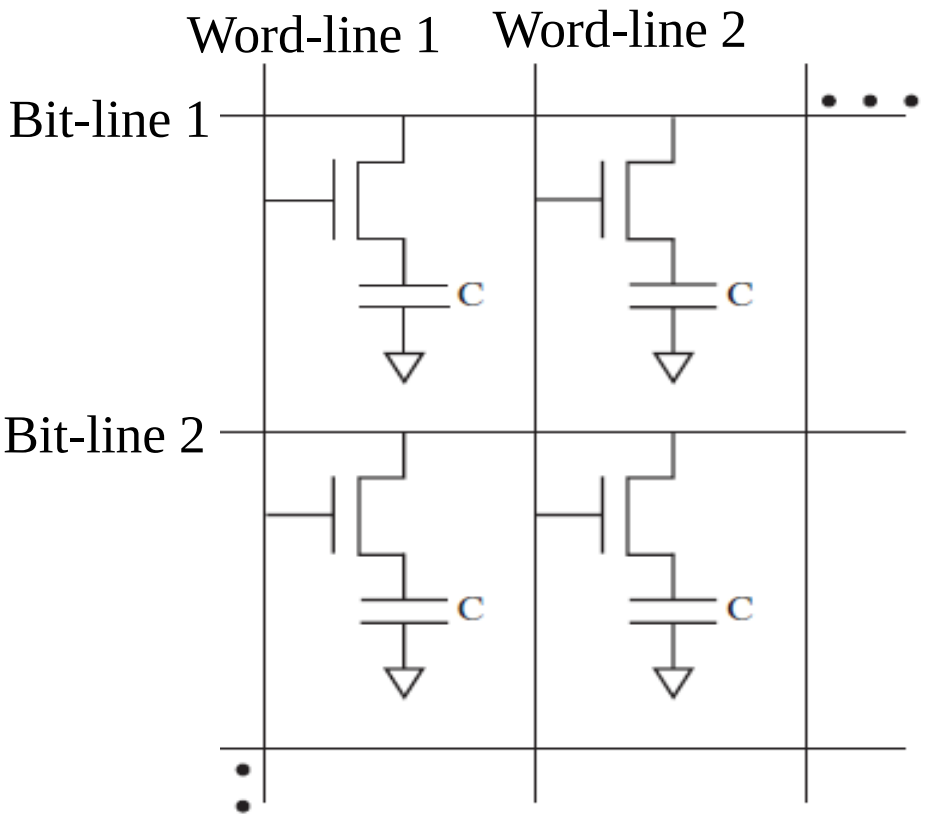
6.16.1 SRAM

>Fastest among all memories.
>Totally CMOS compatible.
>Cost per bit is the highest-- uses 6 transistors to store one bit of data.



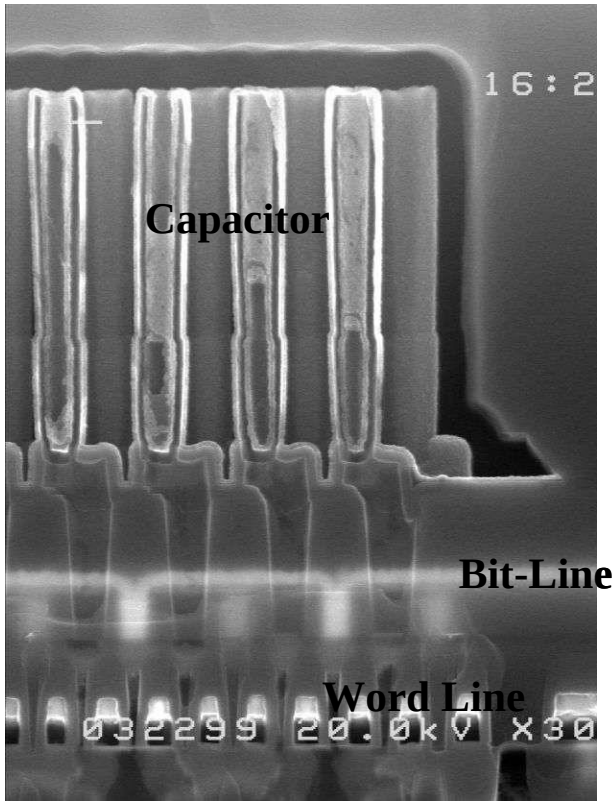


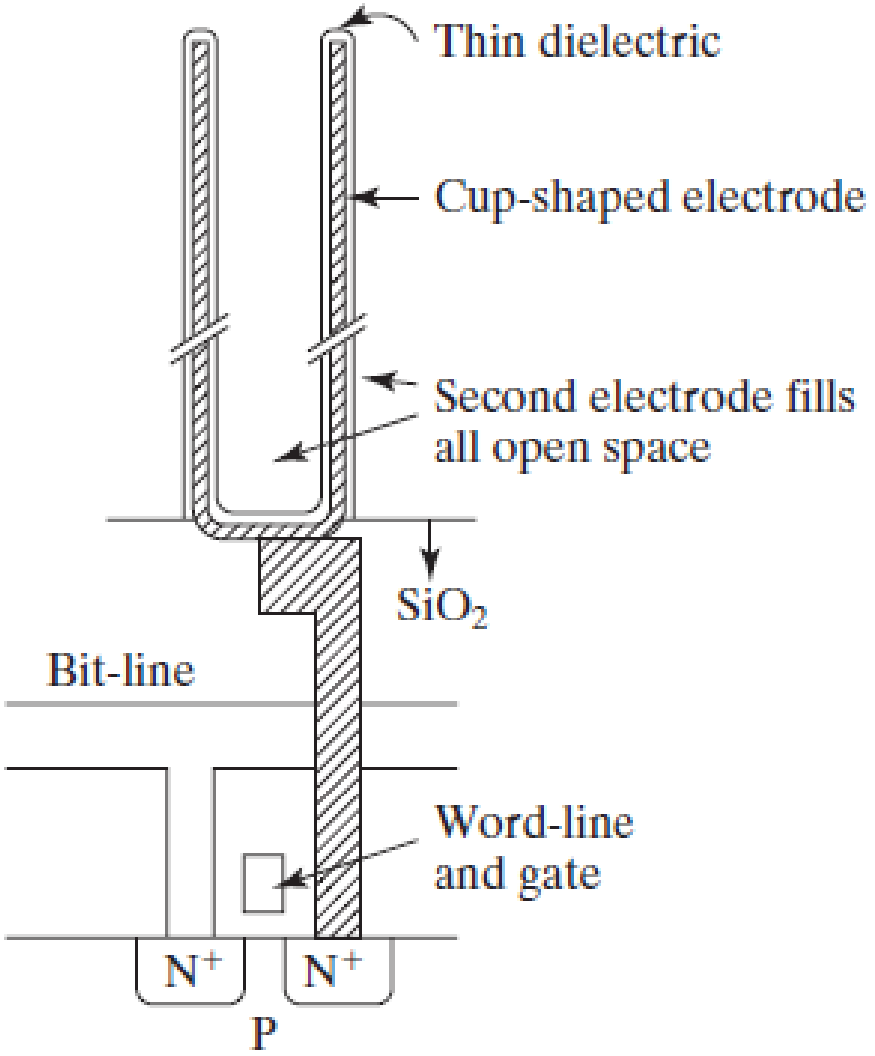
6.16.2 DRAM



- DRAM capacitor can only hold the data (charge) for a limited time because of leakage current.
- Needs refresh.
- Needs ~10fF C in a small and shrinking area -- for refresh time and error rate.

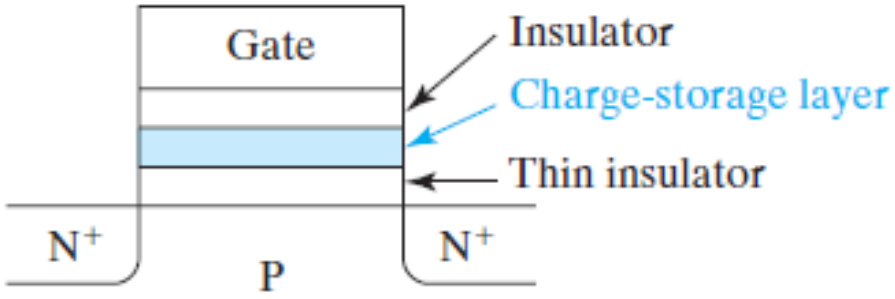
6.16.2 DRAM capacitor technology

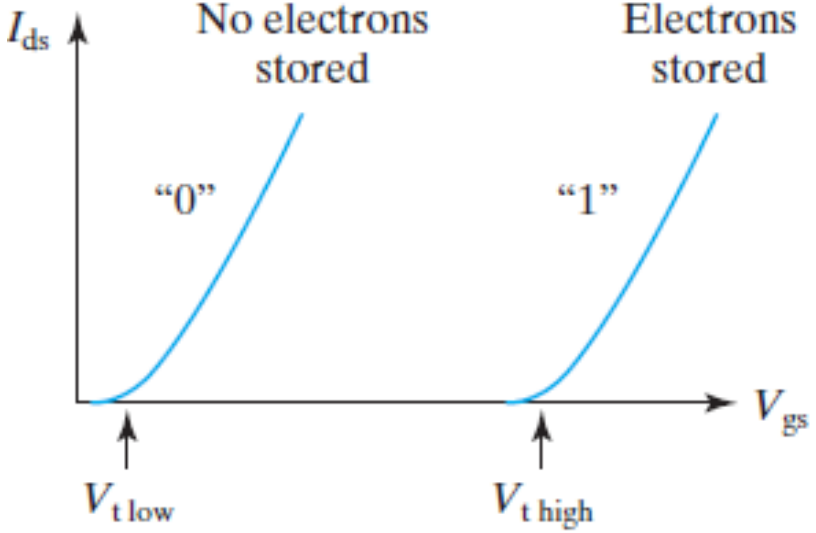


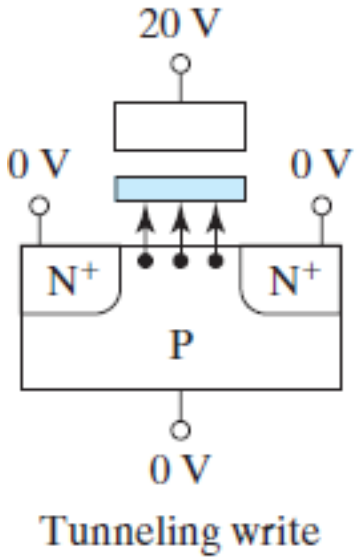


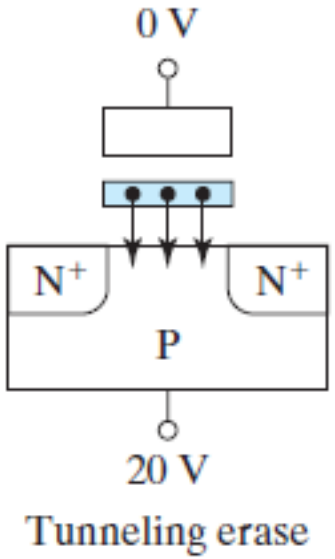
Stacked capacitor* and *Trench capacitor

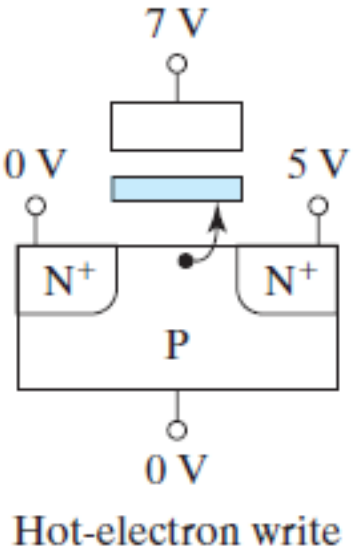
6.16.3 Nonvolatile (Flash) Memory





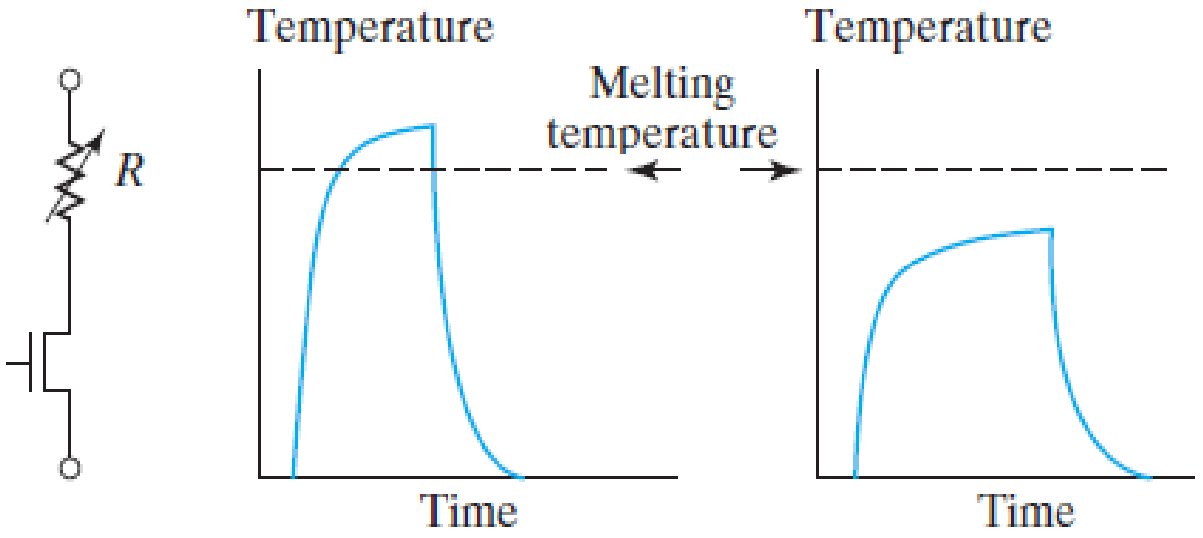






- **Floating gate (poly-Si)**
- **Charge trap (SONOS)**
- **Nanocrystal**

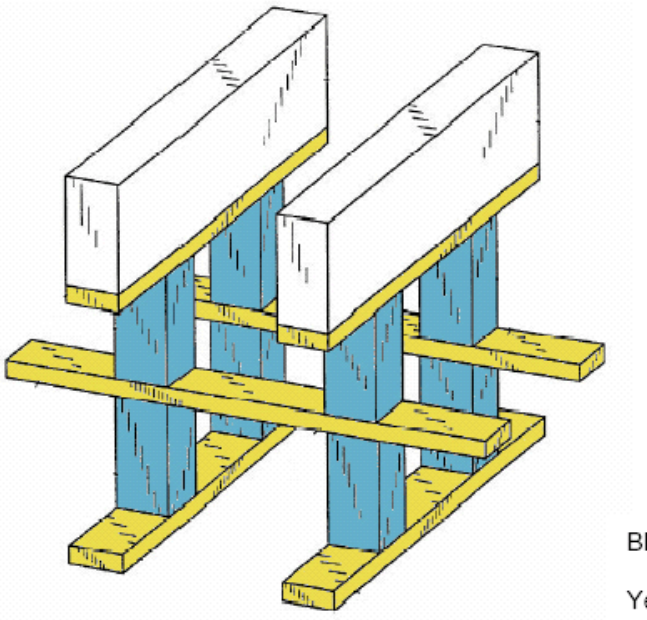
Phase Change Memory



Alloy of Ge, Sb, Te has high resistivity in amorphous phase and low resistivity in polycrystalline phase.

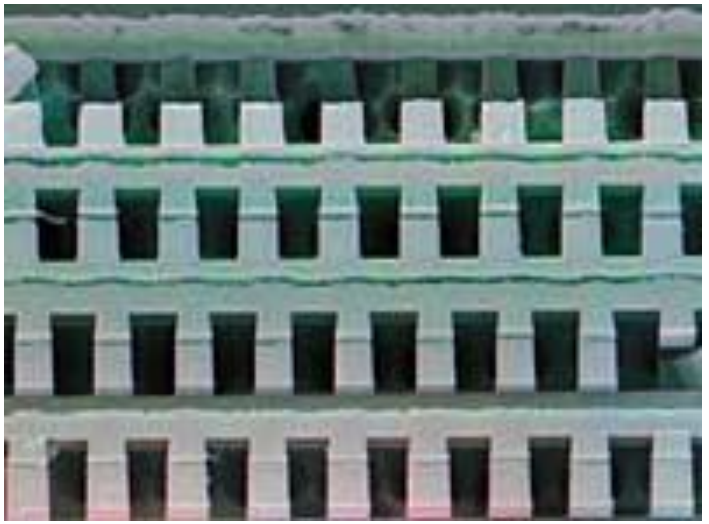
3D (Multi-layer) Memory

- Epitaxy from seed windows can produce Si layers.
- Ideally memory element is simple and does not need single-crystalline material.



Blue = Device

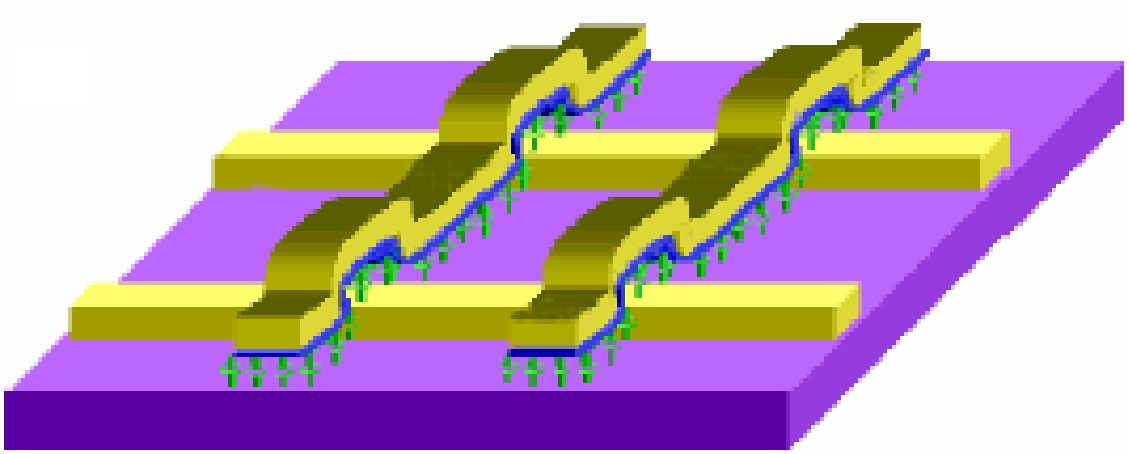
Yellow = Conductor



Resistive Memory (RRAM)

-- Organic, inorganic, metallic.. material

-- Future extension to 3-D



6.17 Chapter Summary

- ***propagation delay***

$$\tau_d \approx \frac{CV_{dd}}{4}\left(\frac{1}{I_{onN}} + \frac{1}{I_{onP}}\right)$$

- ***Power Consumption***

$$P = kCV_{dd}^2 f + V_{dd} I_{off}$$

- ***body effect***

$$\boxed{V_t(V_{sb}) = V_{t0} + \alpha V_{sb}}$$ for steep retrograde body doping

$$\alpha = 3T_{oxe} / W_{dmax}$$

6.17 Chapter Summary

- ***basic I_{ds} model***

$$I_{ds} = \frac{W}{L} C_{oxe} \mu_s \left(V_{gs} - V_t - \frac{m}{2} V_{ds}\right) V_{ds}$$

$$m = 1 + 3T_{oxe} / W_{dmax} \approx 1.2$$

• Small α and m are desirable. Therefore, small T_{oxe} is good. Ch.7 shows that large W_{dmax} is not acceptable.

• CMOS circuit speed is determined by CV_{dd}/I_{dsat}, and its power by $CV_{dd}^2 f + V_{dd} I_{off}$.

6.17 Chapter Summary

IV characteristics can be divided into a ***linear region*** and a ***saturation region.***

I_{ds} saturates at:

$$V_{dsat} = \frac{V_{gs} - V_t}{m}$$

$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_s (V_{gs} - V_t)^2$$

transconductance:

$$g_{msat} = \frac{W}{mL} C_{oxe} \mu_s (V_{gs} - V_t)$$

Considering ***velocity saturation,***

$$V_{dsat} = \left(\frac{m}{V_{gs} - V_t} + \frac{1}{\mathcal{E}_{sat} L} \right)^{-1}$$

$$I_{dsat} = \frac{long\text{-}channel\ I_{dsat}}{1 + \frac{V_{gs} - V_t}{m \mathcal{E}_{sat} L}}$$

6.17 Chapter Summary

- At very small L $I_{dsat} = Wv_{sat}C_{oxe}(V_{gs} - V_t)$

- Velocity overshoot can lift v_{sat}, but source velocity limit sets a similar top over I_{dsat}.

$$I_{dsat} = WBv_{thx}C_{oxe}(V_{gs} - V_t)$$

- Intrinsic voltage gain is g_{msat}/g_{ds}

- High f_T and f_{MAX} need low $R_{in} = R_{g-electrode} + R_{ii}$

$$R_{ii} \propto \frac{V_{ds}}{I_{ds}} \qquad R_{g-electrode} \propto N_f^{\,2}$$

- Noise arises from the channel, gate, substrate thermal noises, and the flicker noise.

6.17 Chapter Summary

SRAM, DRAM, Nonvolatle memory

	Keep Data Without Power?	Cell Size and Cost/bit	Rewrite Cycles	Write-One-byte Speed	Compatible with Basic CMOS Manufacturing	Main Applications
SRAM	No	Large	Unlimited	Fast	Totally	Embedded in logic chips
DRAM	No	Small	Unlimited	Fast	Need modifications	Stand-alone chips and embedded
Flash memory	Yes	Smallest	Limited	Slow	Need extensive modifications	Nonvolatile storage stand-alone