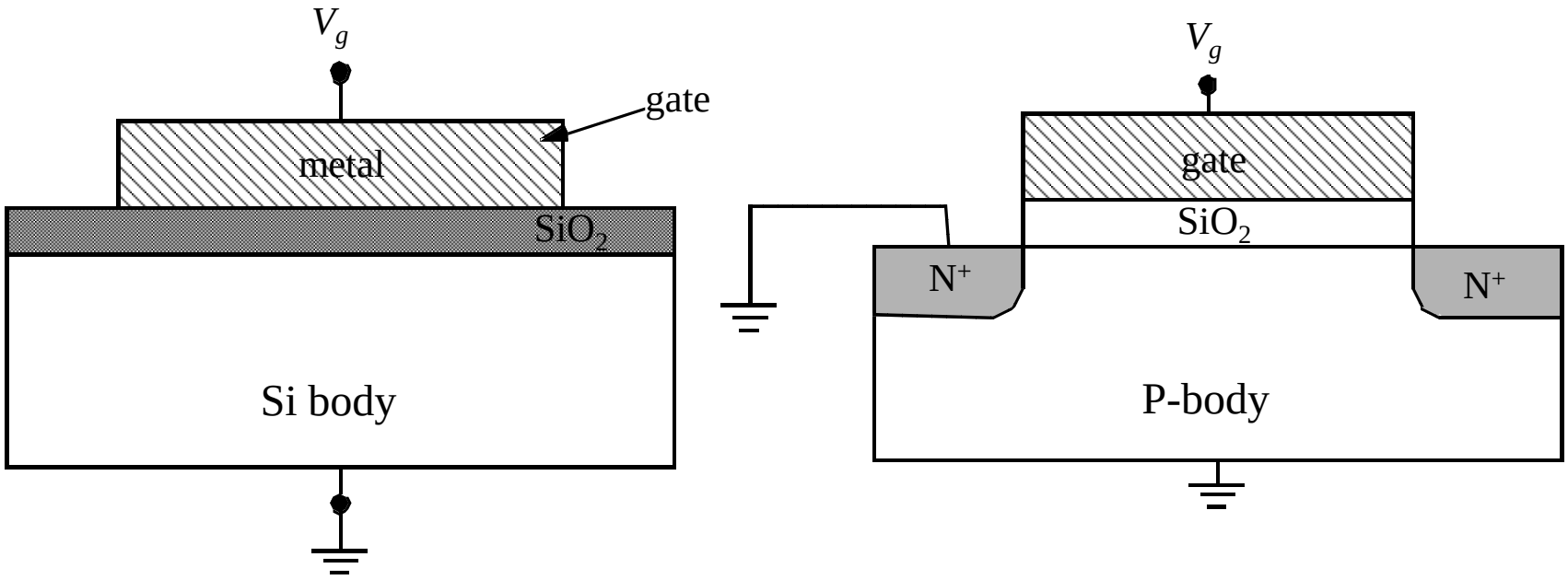
Chapter 5 MOS Capacitor

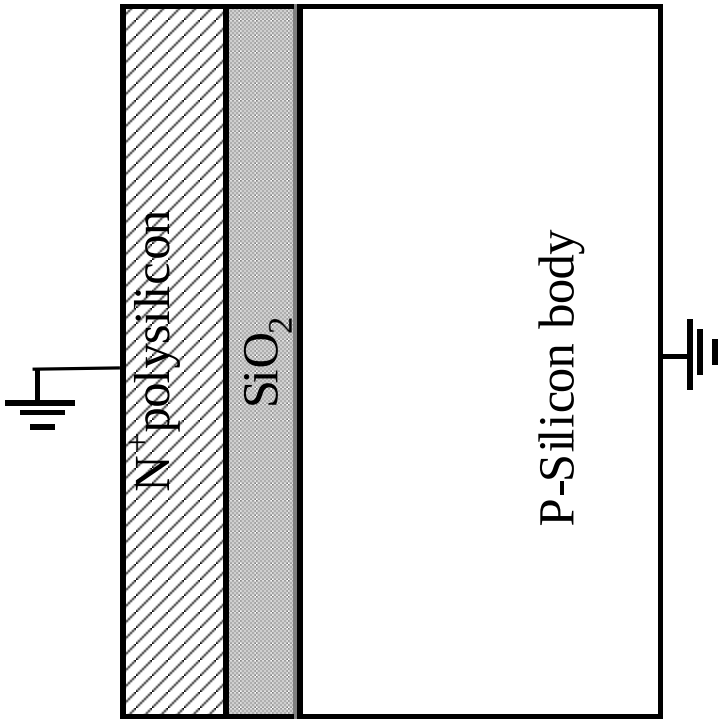
MOS: Metal-Oxide-Semiconductor

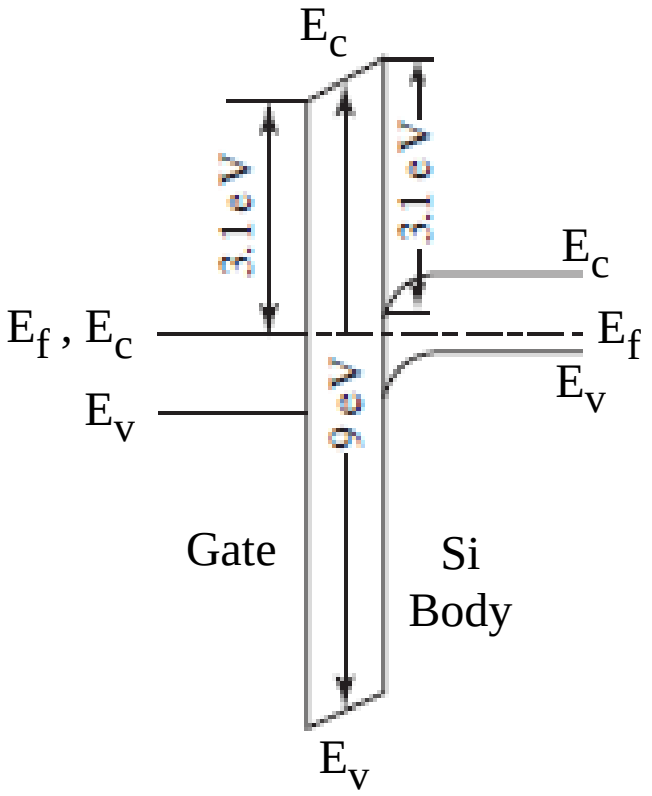


MOS capacitor

MOS transistor

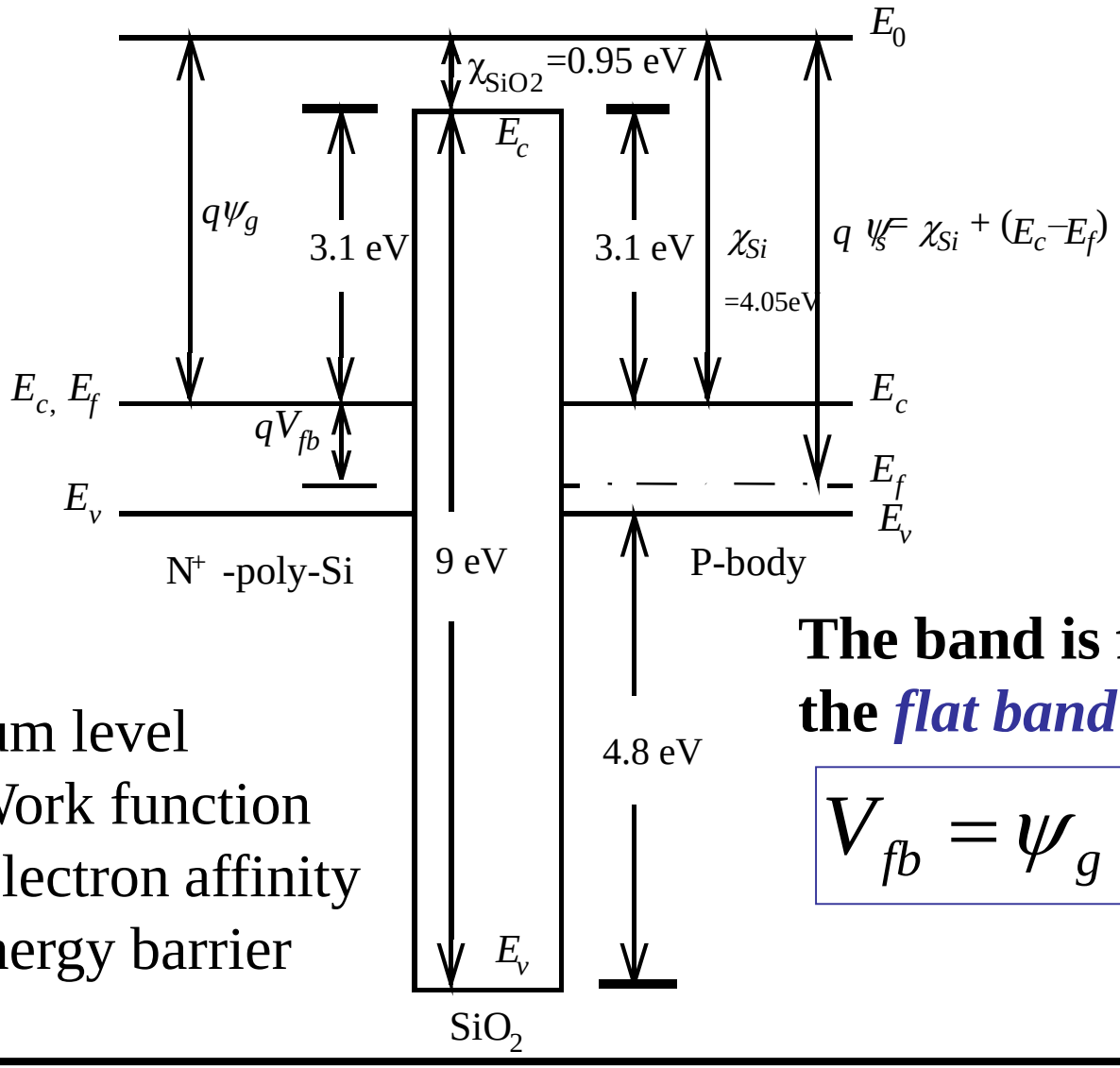
Chapter 5 MOS Capacitor





This energy-band diagram for $V_g = 0$ is not the simplest one.

5.1 Flat-band Condition and Flat-band Voltage



E_0 : Vacuum level

$E_0 - E_f$: Work function

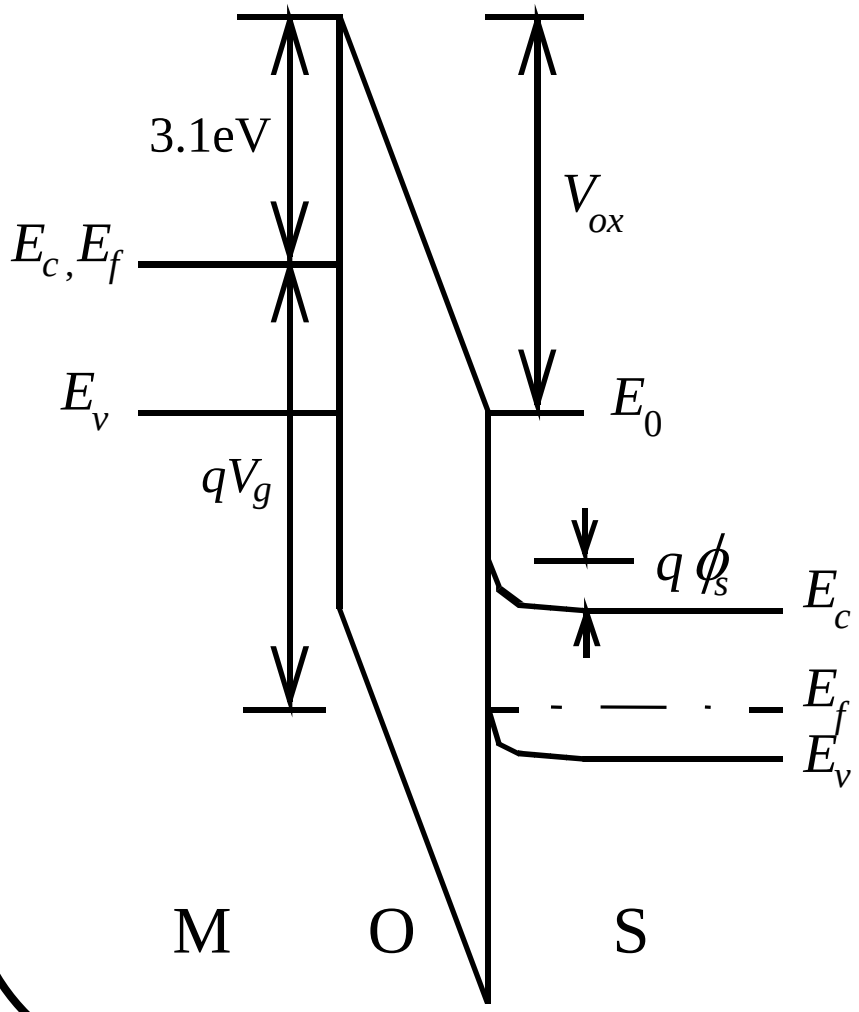
$E_0 - E_c$: Electron affinity

Si/SiO_2 energy barrier

The band is flat at the *flat band voltage*.

$$V_{fb} = \psi_g - \psi_s$$

5.2 Surface Accumulation



Make $V_g < V_{fb}$

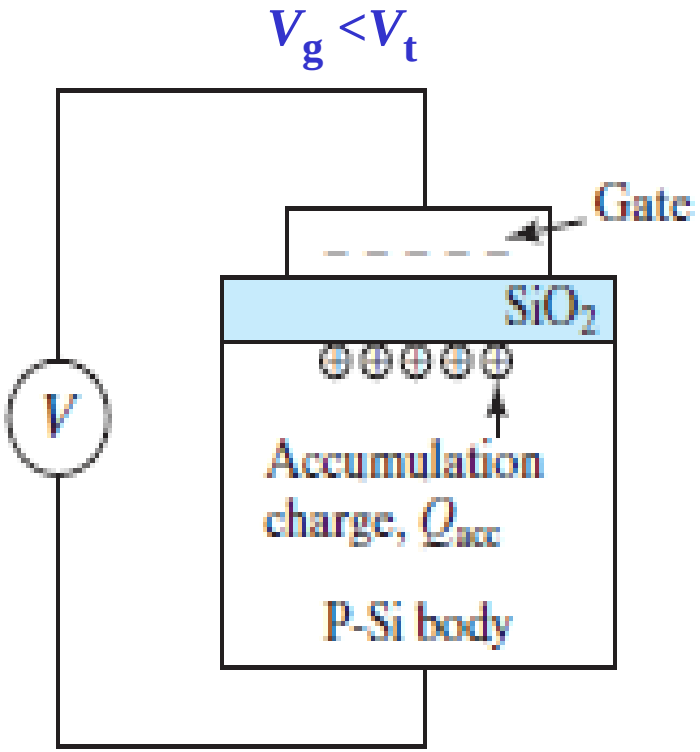
$$V_g = V_{fb} + \phi_s + V_{ox}$$

ϕ_s : surface potential, band bending

V_{ox}: voltage across the oxide

ϕ_s is negligible when the surface is in accumulation.

5.2 Surface Accumulation



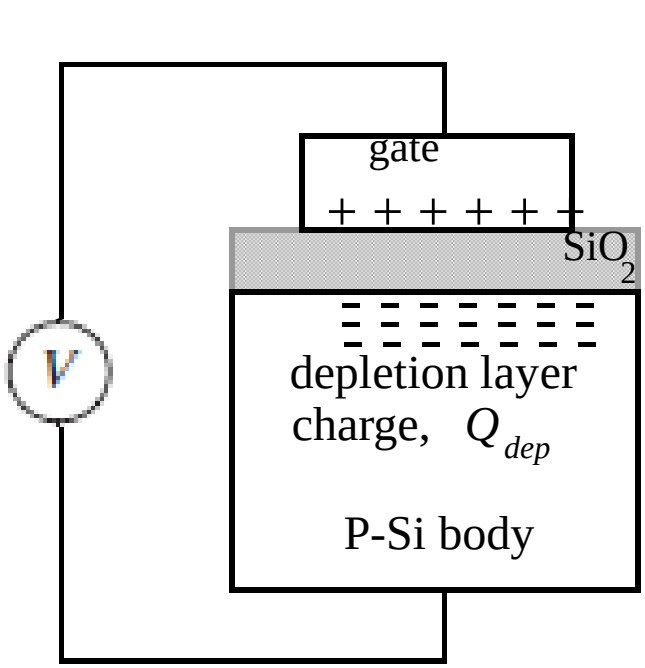
$$V_{ox} = V_g - V_{fb}$$

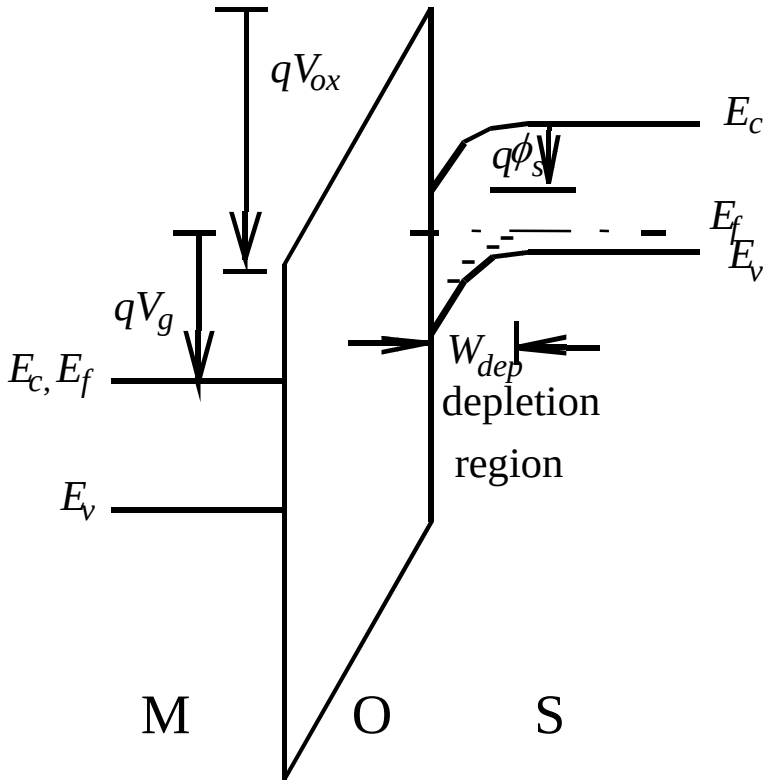
Gauss's Law $\rightarrow V_{ox} = -Q_{acc} / C_{ox}$

$$Q_{acc} = -C_{ox}(V_g - V_{fb})$$

$$V_{ox} = -Q_s / C_{ox}$$

5.3 Surface Depletion ($V_g > V_{fb}$)





$$V_{ox} = -\frac{Q_s}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}} = \frac{qN_a W_{dep}}{C_{ox}} = \frac{\sqrt{qN_a 2\varepsilon_s \phi_s}}{C_{ox}}$$

5.3 Surface Depletion

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \phi_s + \frac{\sqrt{qN_a 2\varepsilon_s \phi_s}}{C_{ox}}$$

This equation can be solved to yield ϕ_s .

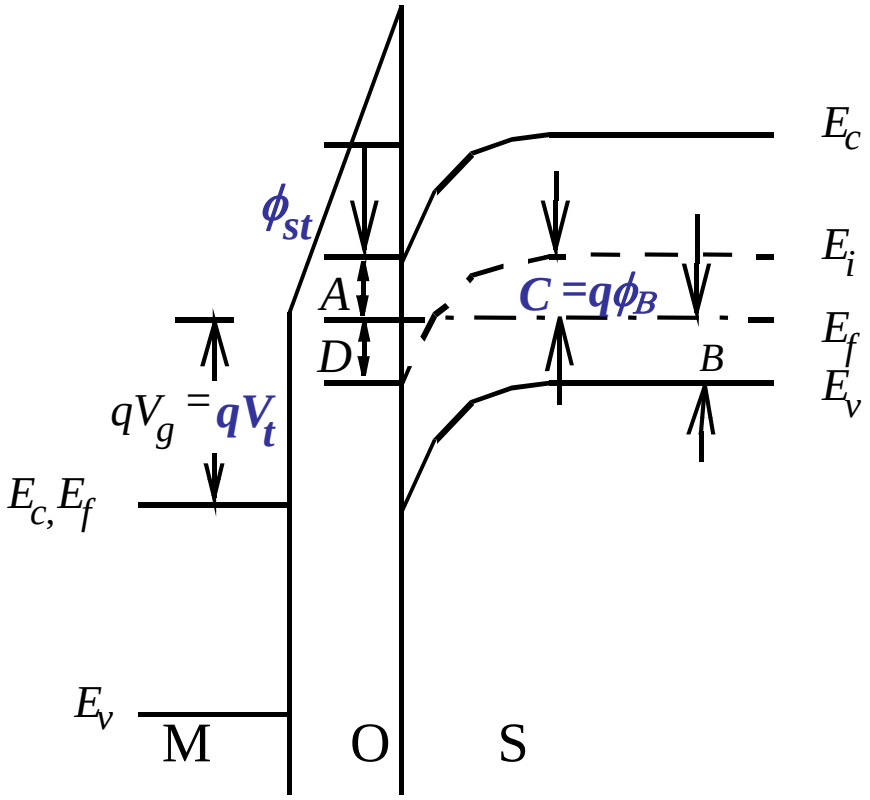
5.4 Threshold Condition and Threshold Voltage

Threshold (of inversion):

$n_s = N_a$, or

$(E_c - E_f)_{surface} = (E_f - E_v)_{bulk}$, or

⇒ $A = B$, and $C = D$



$$\phi_{st} = 2\phi_B = 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

$$q\phi_B = \frac{E_g}{2} - (E_f - E_v)\big|_{bulk} = \frac{kT}{q}\ln\left(\frac{N_v}{n_i}\right) - \frac{kT}{q}\ln\left(\frac{N_v}{N_a}\right) = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

Threshold Voltage

$$V_g = V_{fb} + \varphi_s + V_{ox}$$

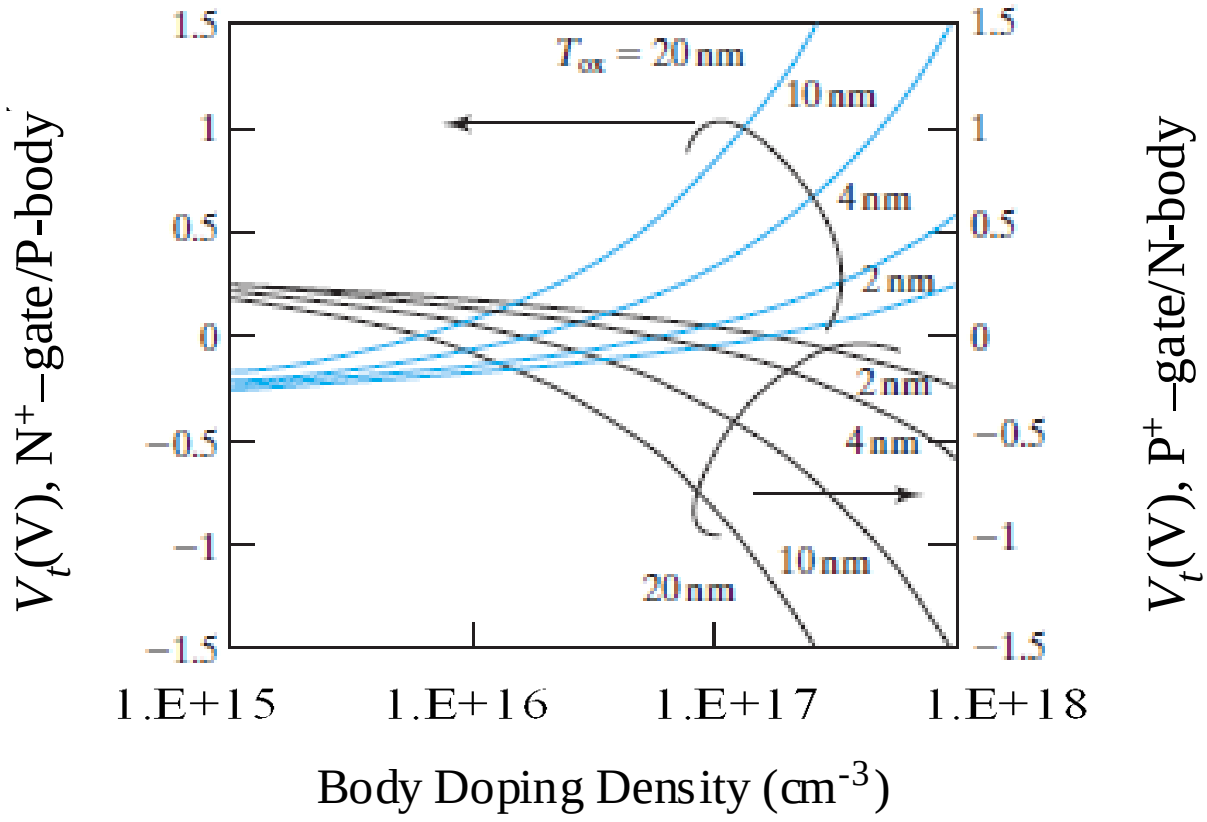
At threshold,

$$\varphi_{st} = 2\phi_B = 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$$

$$V_{ox} = \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

$$V_t = V_g \text{ at threshold} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

Threshold Voltage



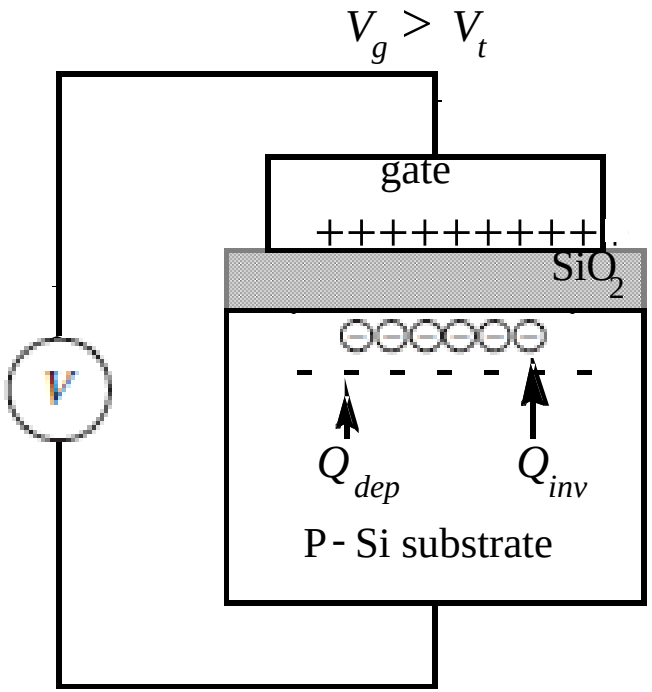
$$V_t = V_{fb} \pm 2\phi_B \pm \frac{\sqrt{qN_{sub}\,2\varepsilon_s\,2\phi_B}}{C_{ox}}$$

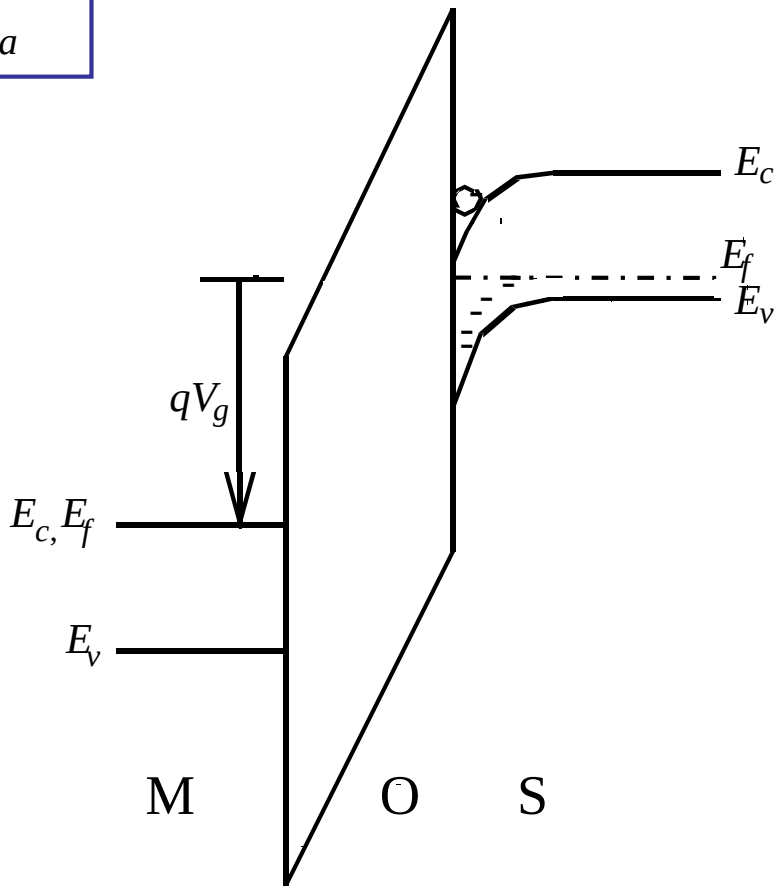
+ for P-body,
– for N-body

5.5 Strong Inversion–Beyond Threshold

$V_g > V_t$

$$W_{dep} = W_{dmax} = \sqrt{\frac{2\varepsilon_s 2\phi_B}{qN_a}}$$

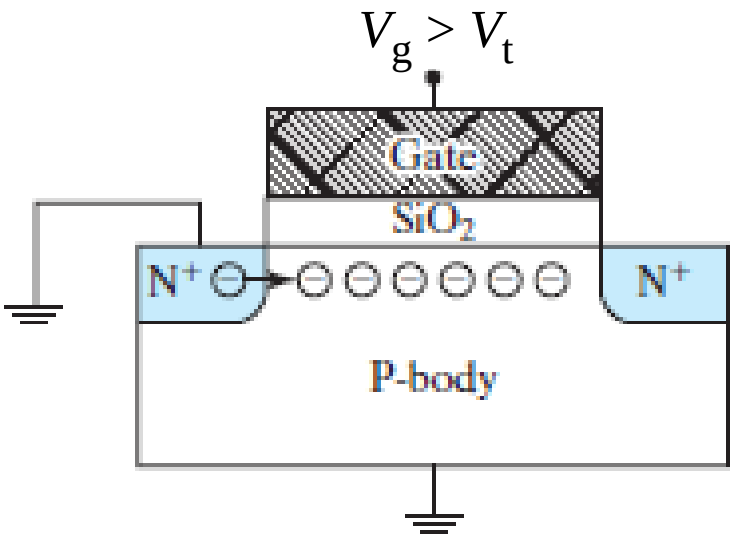


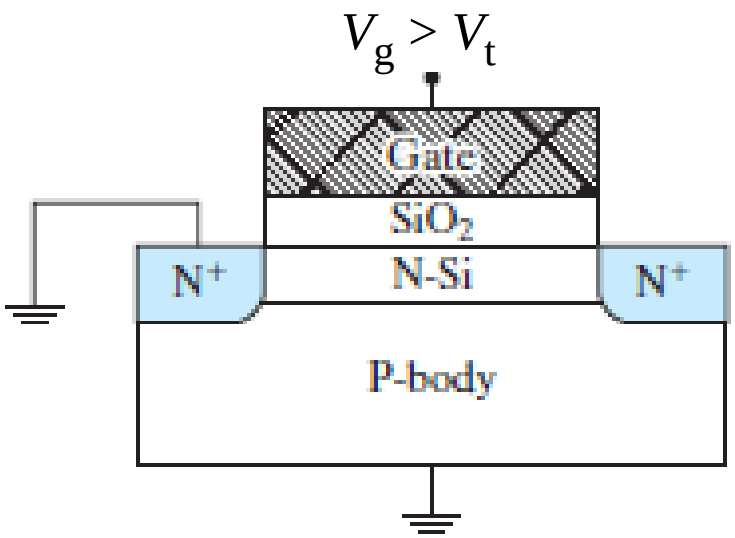


Inversion Layer Charge, Q_{inv} (C/cm²)

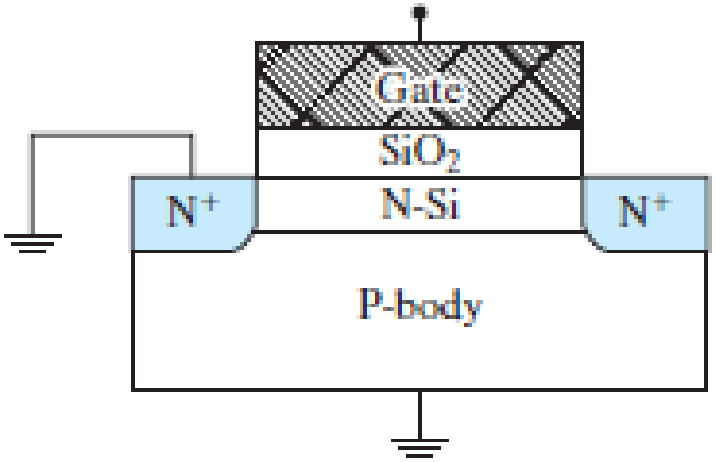
$$V_g = V_{fb} + 2\phi_B - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

$$= V_t - \frac{Q_{inv}}{C_{ox}} \qquad \therefore \quad \boxed{Q_{inv} = -C_{ox}(V_g - V_t)}$$





5.5.1 Choice of V_t and Gate Doping Type

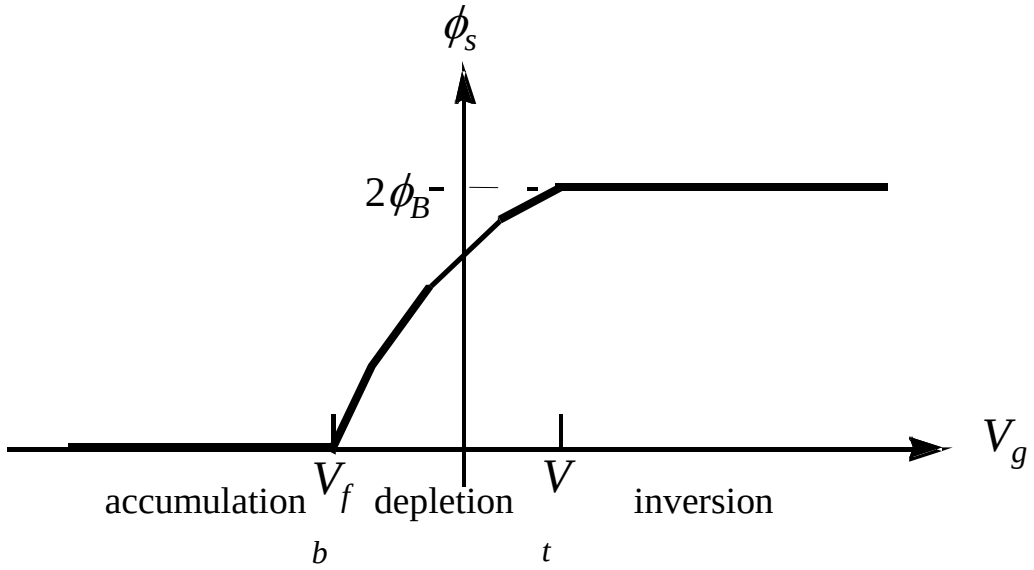


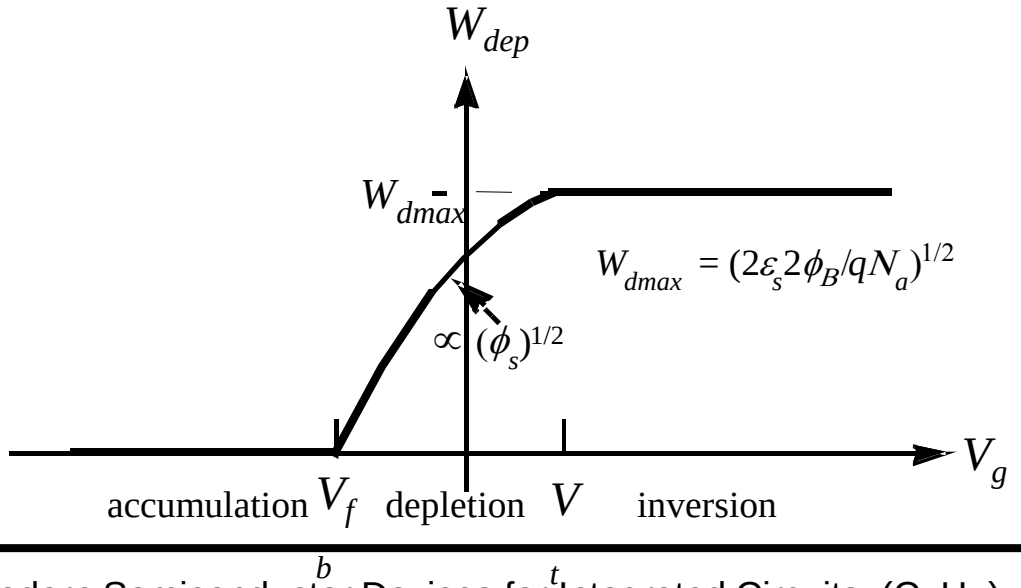
V_t is generally set at a small positive value so that, at V_g = 0, the transistor does not have an inversion layer and current does not flow between the two N^+ regions

• P-body is normally paired with N^+-gate to achieve a small positive threshold voltage.

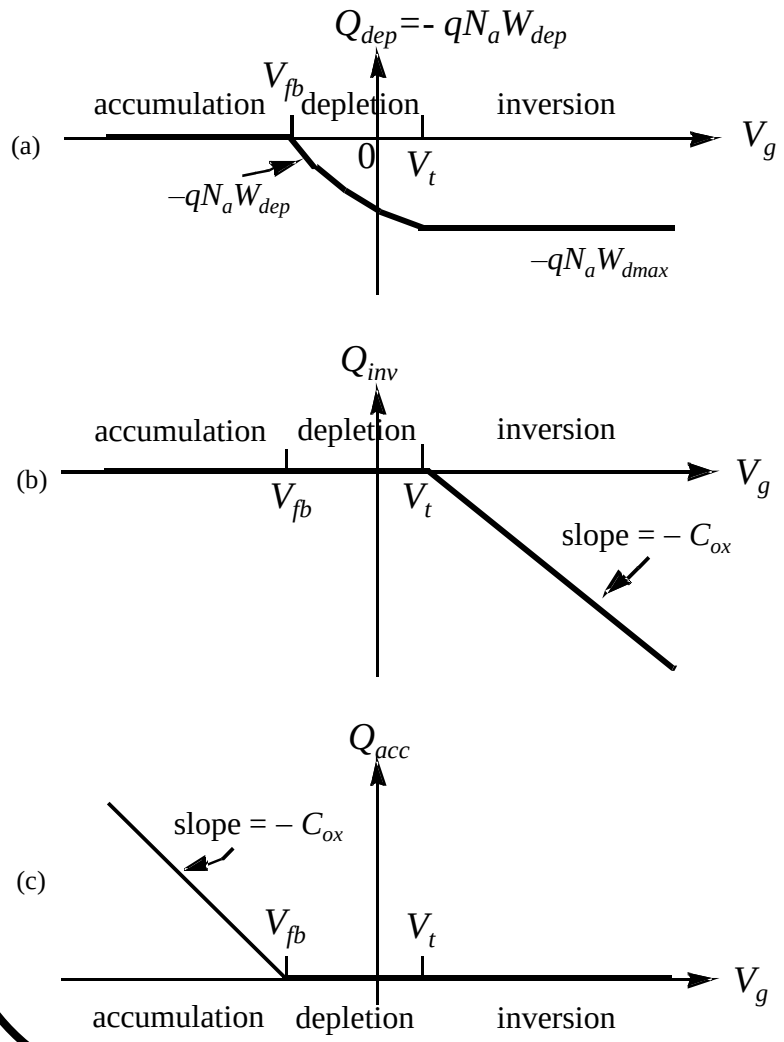
• N-body is normally paired with P^+-gate to achieve a small negative threshold voltage.

Review : Basic MOS Capacitor Theory



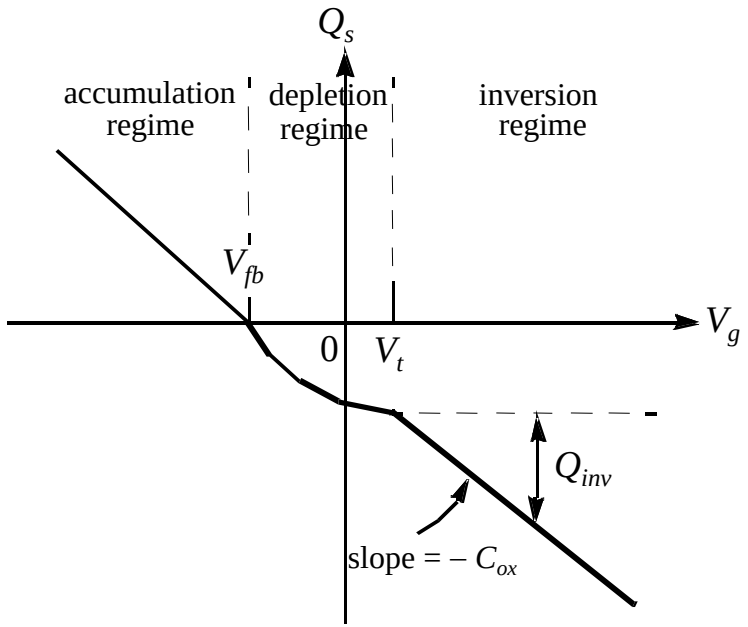


Review : Basic MOS Capacitor Theory

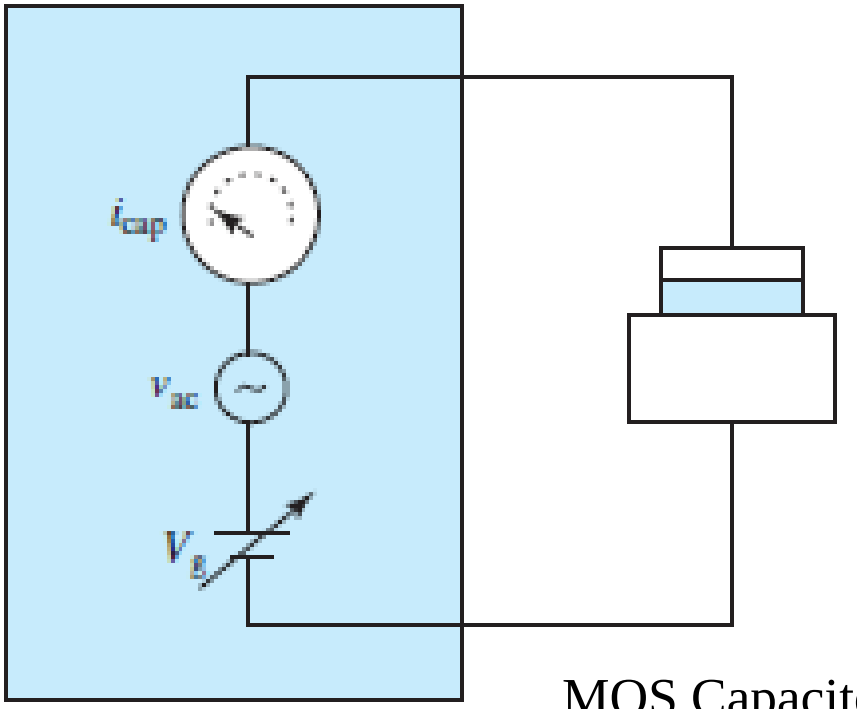


total substrate charge, Q_s

$$Q_s = Q_{acc} + Q_{dep} + Q_{inv}$$



5.6 MOS CV Characteristics



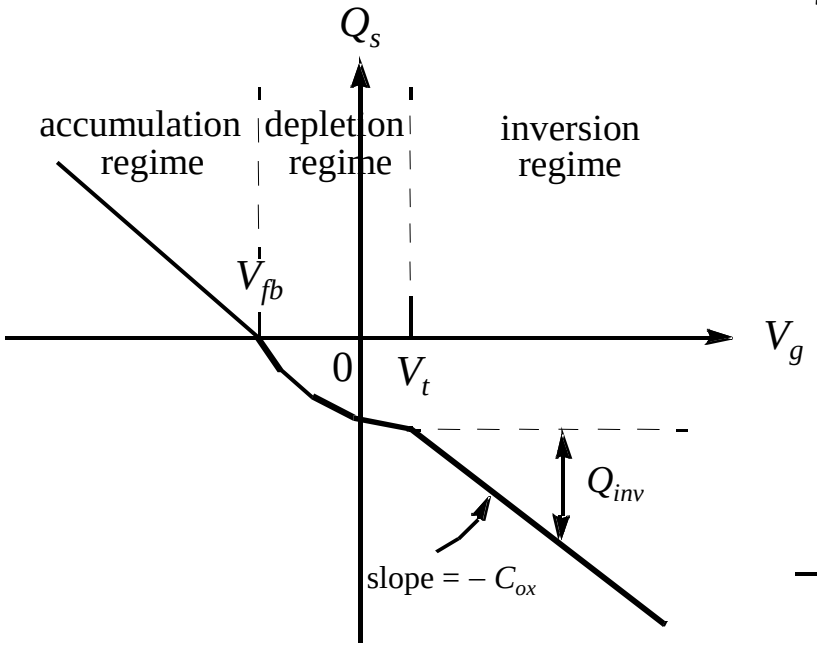
C-V Meter

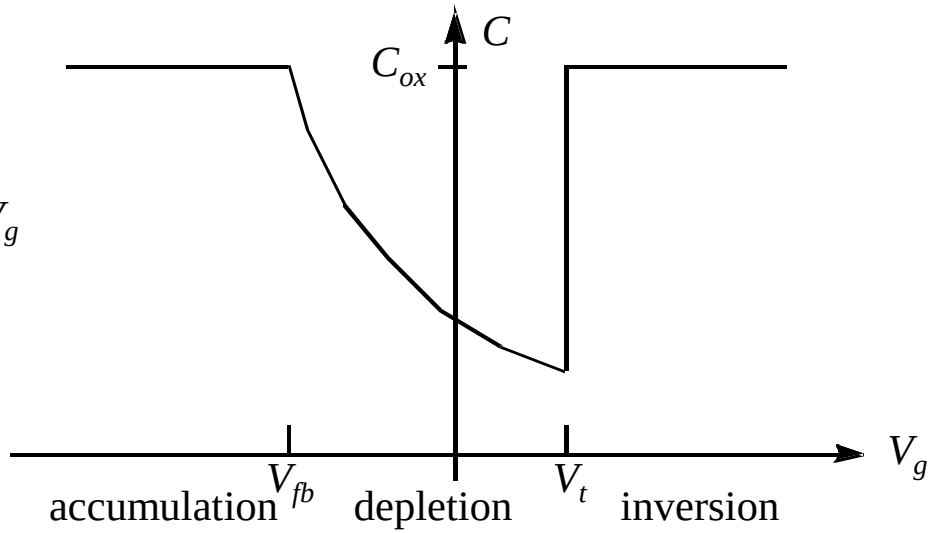
MOS Capacitor

$$C = \frac{dQ_g}{dV_g} = -\frac{dQ_s}{dV_g}$$

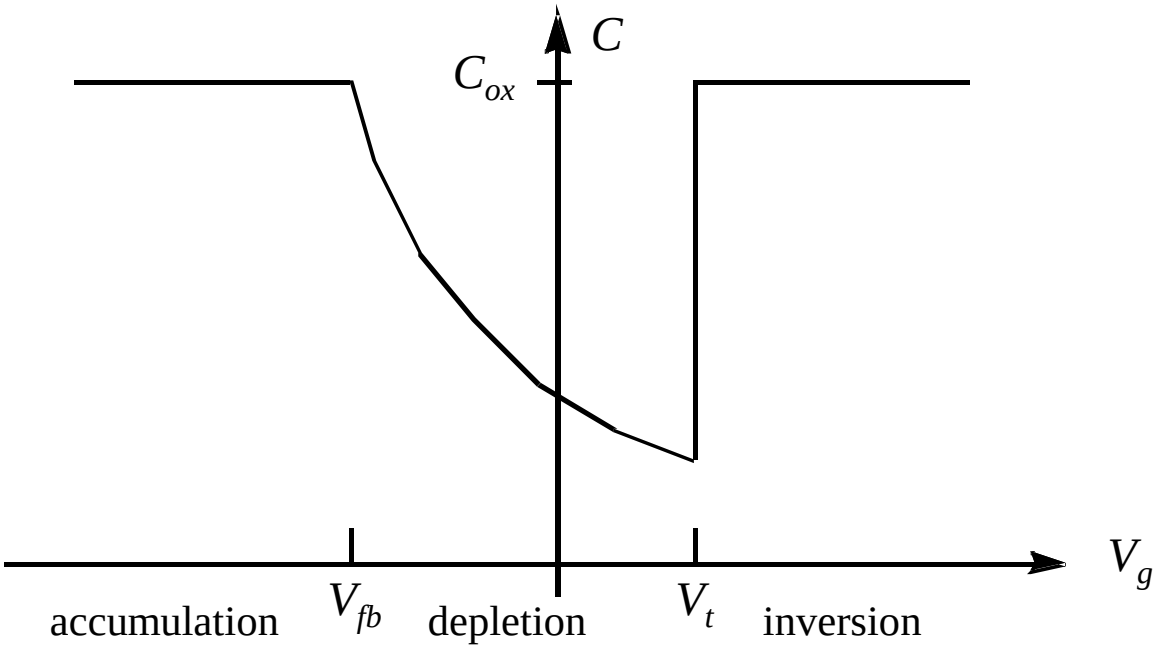
5.6 MOS CV Characteristics

$$C = \frac{dQ_g}{dV_g} = -\frac{dQ_s}{dV_g}$$





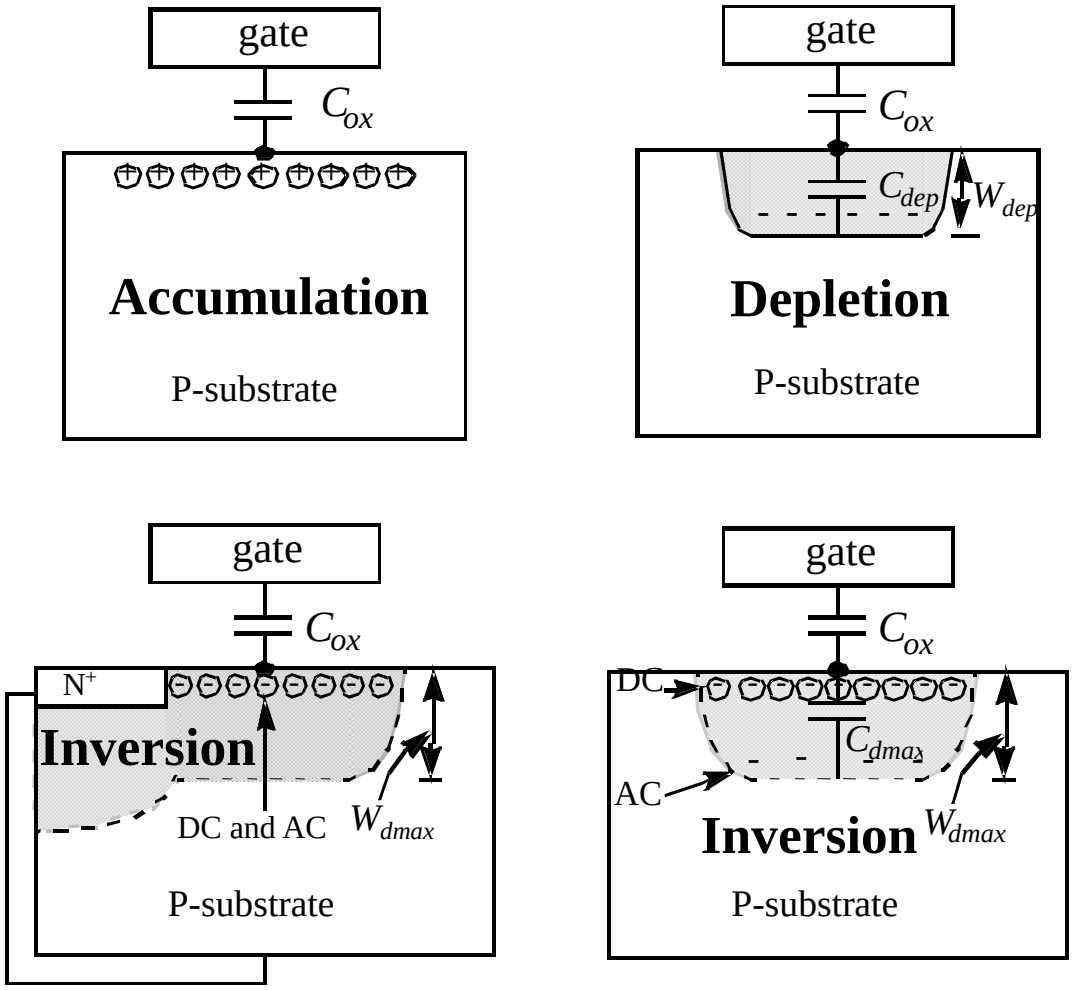
CV Characteristics



In the depletion regime: $$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

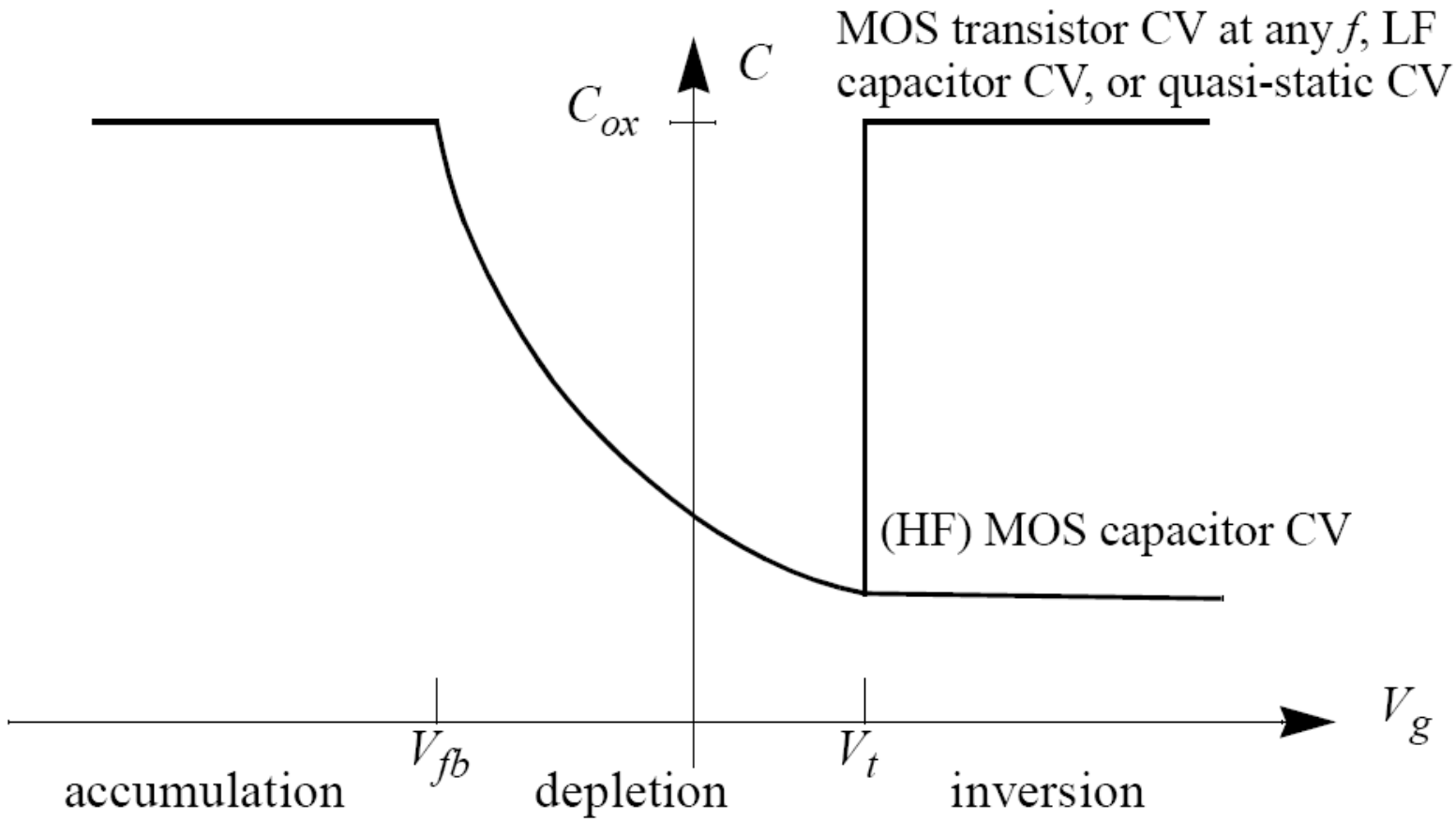
$$\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}}$$

Supply of Inversion Charge May be Limited

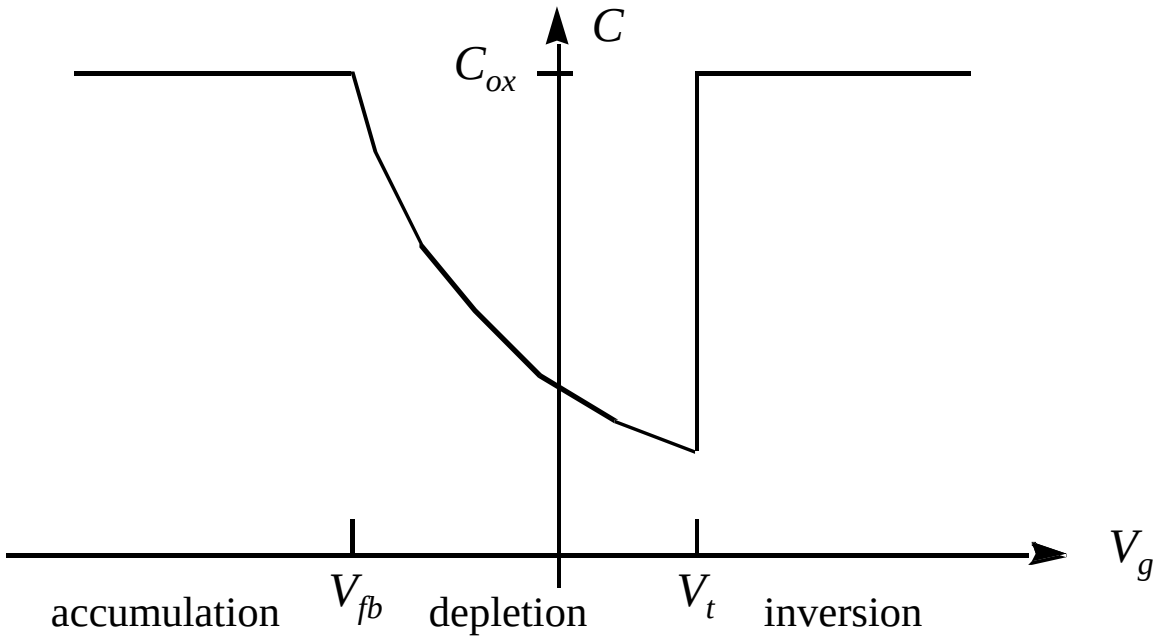


In each case, C = ?

Capacitor and Transistor CV (or HF and LF CV)

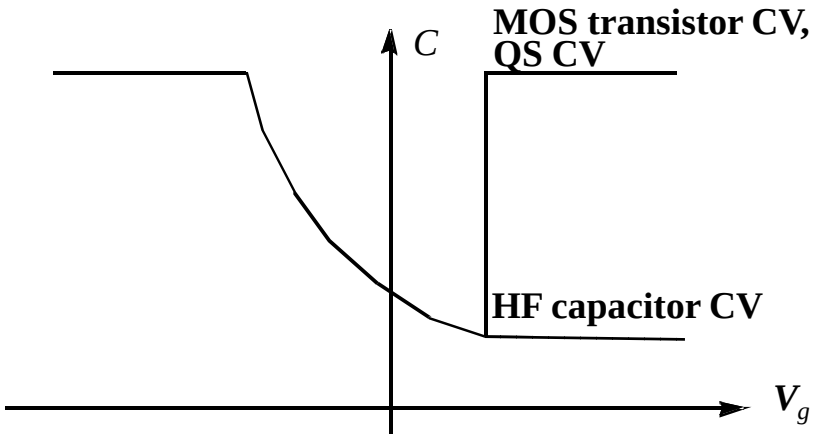


Quasi-Static CV of MOS Capacitor



The quasi-static CV is obtained by the application of a slow linear-ramp voltage (< 0.1V/s) to the gate, while measuring I_g with a very sensitive DC ammeter. C is calculated from $I_g = C \cdot dV_g/dt$. This allows sufficient time for Q_{inv} to respond to the slow-changing V_g .

EXAMPLE : CV of MOS Capacitor and Transistor



Does the QS CV or the HF capacitor CV apply?

(1) MOS transistor, 10kHz. *(Answer: QS CV).*

(2) MOS transistor, 100MHz. *(Answer: QS CV).*

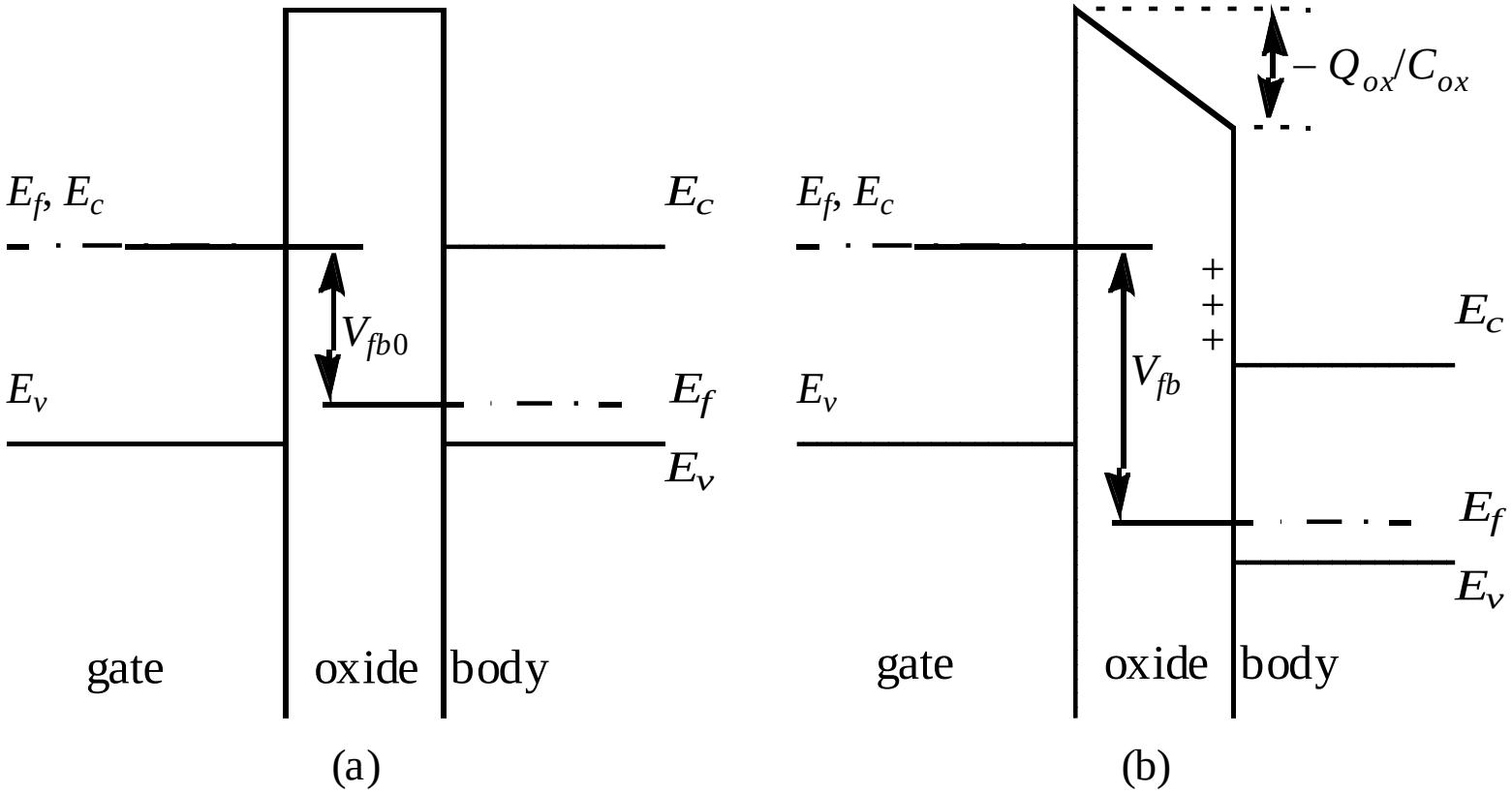
(3) MOS capacitor, 100MHz. *(Answer: HF capacitor CV).*

(4) MOS capacitor, 10kHz. *(Answer: HF capacitor CV).*

(5) MOS capacitor, slow V_g ramp. *(Answer: QS CV).*

(6) MOS transistor, slow V_g ramp. *(Answer: QS CV).*

5.7 Oxide Charge–A Modification to V_{fb} and V_t



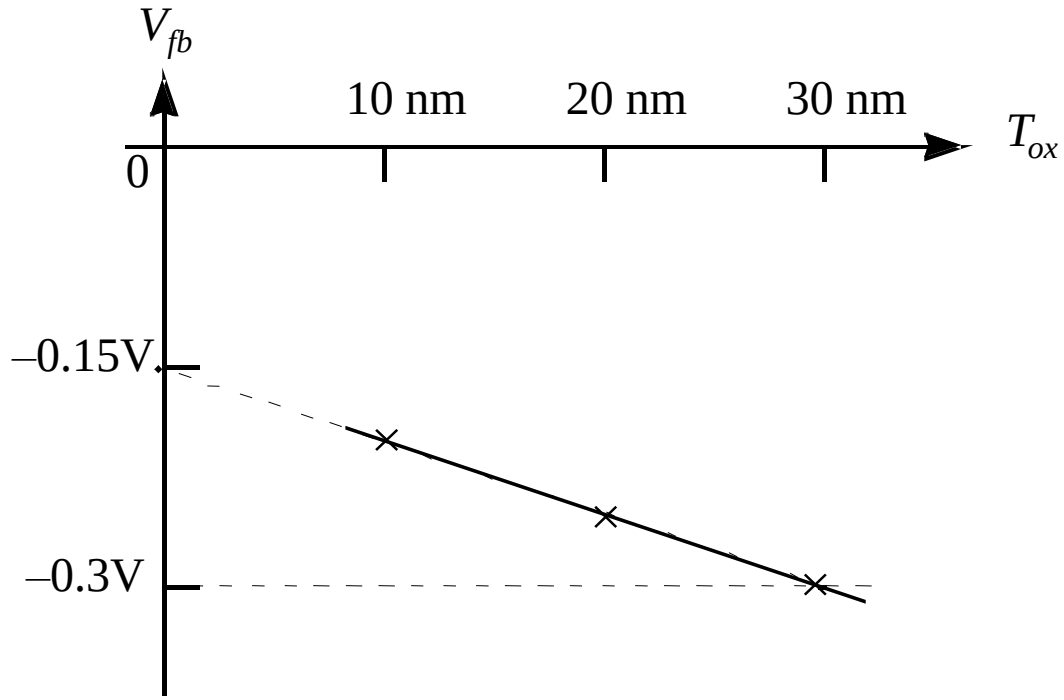
$$V_{fb} = V_{fb0} - Q_{ox}/C_{ox} = \psi_g - \psi_s - Q_{ox}/C_{ox}$$

5.7 Oxide Charge–A Modification to V_{fb} and V_t

Types of oxide charge:

- Fixed oxide charge, Si^+
- Mobile oxide charge, due to Na^+contamination
- Interface traps, neutral or charged depending on Vg.
- Voltage/temperature stress induced charge and traps--a reliability issue

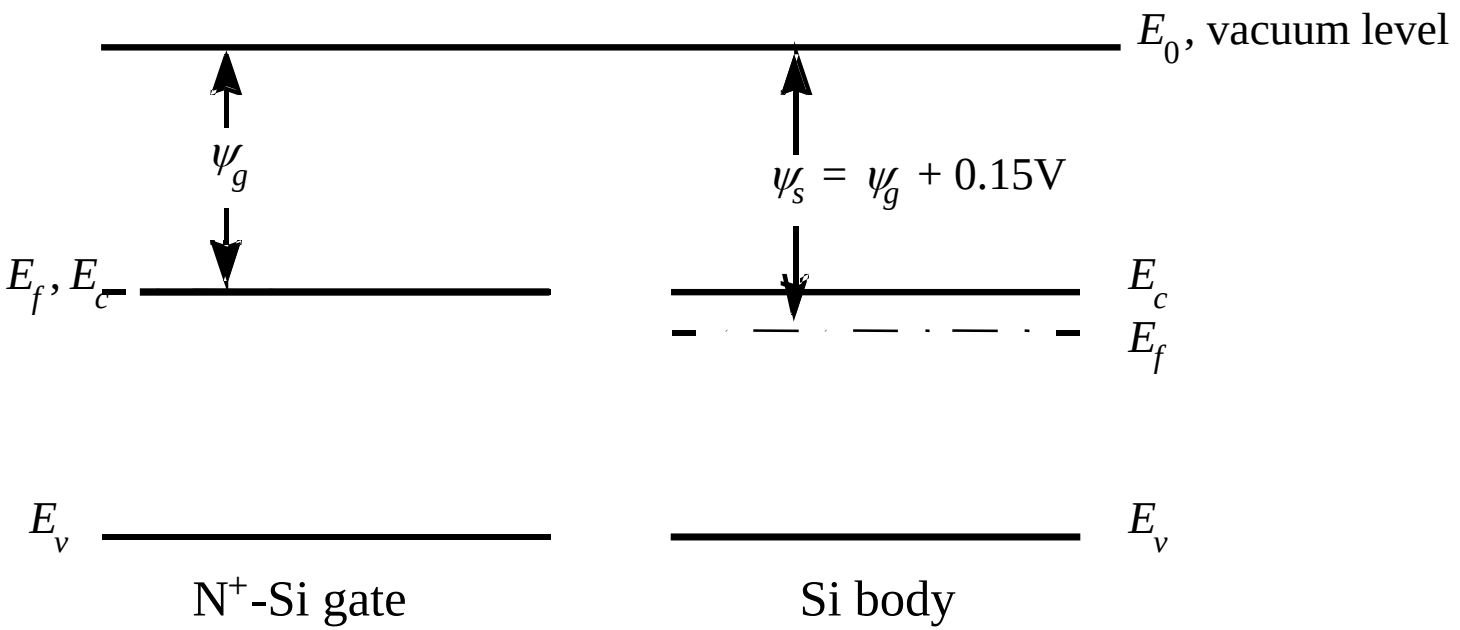
EXAMPLE: *Interpret this measured V_{fb} dependence on oxide thickness. The gate electrode is N^+ poly-silicon.*



What does it tell us? Body work function? Doping type? Other?

Solution: $V_{fb} = \psi_g - \psi_s - Q_{ox}T_{ox} / \varepsilon_{ox}$

$$\textit{from intercept} \longrightarrow \psi_g - \psi_s = -0.15\,\text{V}$$

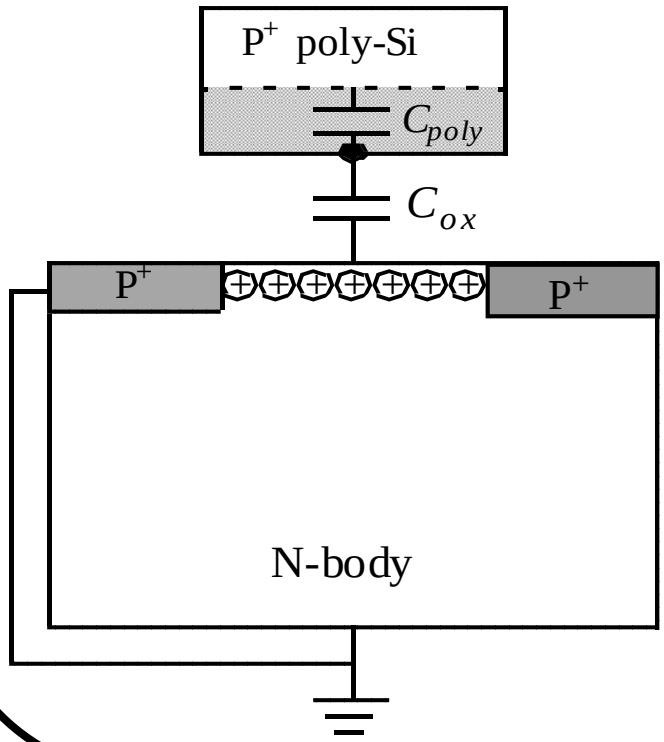


$$\textit{N-type substrate,}\quad N_d = n = N_c e^{-0.15\,\text{eV}/kT} \approx 10^{17}\ \text{cm}^{-3}$$

$$\textit{from slope} \longrightarrow Q_{ox} = 1.7\times10^{-8}\ \text{C/cm}^2$$

5.8 Poly-Silicon Gate Depletion–Effective Increase in T_{ox}

Gauss's Law $W_{dpoly} = \varepsilon_{ox}\mathbf{E}_{ox} / qN_{poly}$



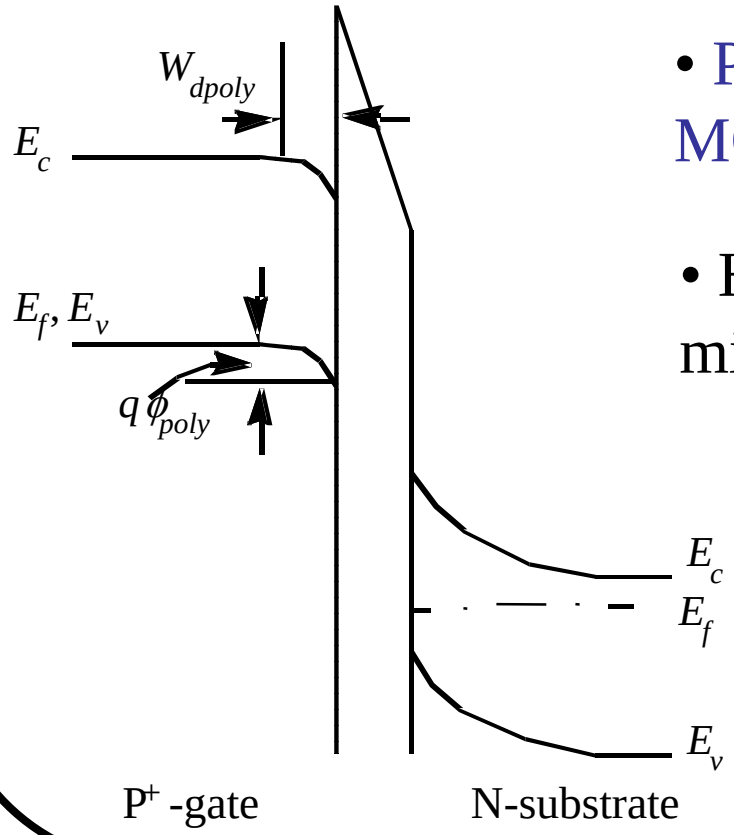
$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{poly}} \right)^{-1} = \left(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{W_{dpoly}}{\varepsilon_s} \right)^{-1}$$

$$= \frac{\varepsilon_{ox}}{T_{ox} + W_{dpoly}/3}$$

If W_{dpoly}= 15 Å, what is the effective increase in T_{ox}?

Effect of Poly-Gate Depletion on Q_{inv}

$$Q_{inv} = C_{ox}(V_g - \phi_{poly} - V_t)$$



- Poly-gate depletion degrades MOSFET current and circuit speed.
- How can poly-depletion be minimized?

EXAMPLE : Poly-Silicon Gate Depletion

V_{ox} , the voltage across a 2 nm thin oxide, is –1 V. The P^+ poly-gate doping is $N_{poly} = 8 \times 10^{19}\ cm^{-3}$ and substrate N_d is $10^{17} cm^{-3}$. Find (a) W_{dpoly} , (b) ϕ_{poly} , and (c) V_g .

Solution:

(a) $$W_{dpoly} = \varepsilon_{ox}\mathcal{E}_{ox} / qN_{poly} = \varepsilon_{ox}V_{ox} / T_{ox}qN_{poly}$$

$$= \frac{3.9 \times 8.85 \times 10^{-14}\,(\mathrm{F/cm}) \times 1\,\mathrm{V}}{2 \times 10^{-7}\,\mathrm{cm} \times 1.6 \times 10^{-19}\,\mathrm{C} \times 8 \times 10^{19}\,\mathrm{cm}^{-3}}$$

$$= 1.3\,\mathrm{nm}$$

EXAMPLE : Poly-Silicon Gate Depletion

(b) $$W_{dpoly} = \sqrt{\frac{2\varepsilon_s \phi_{poly}}{qN_{poly}}}$$

$$\phi_{dpoly} = qN_{poly}W_{dpoly}^2 / 2\varepsilon_s = 0.11\,\text{V}$$

(c) $$V_g = V_{fb} + \phi_{st} + V_{ox} + \phi_{poly}$$

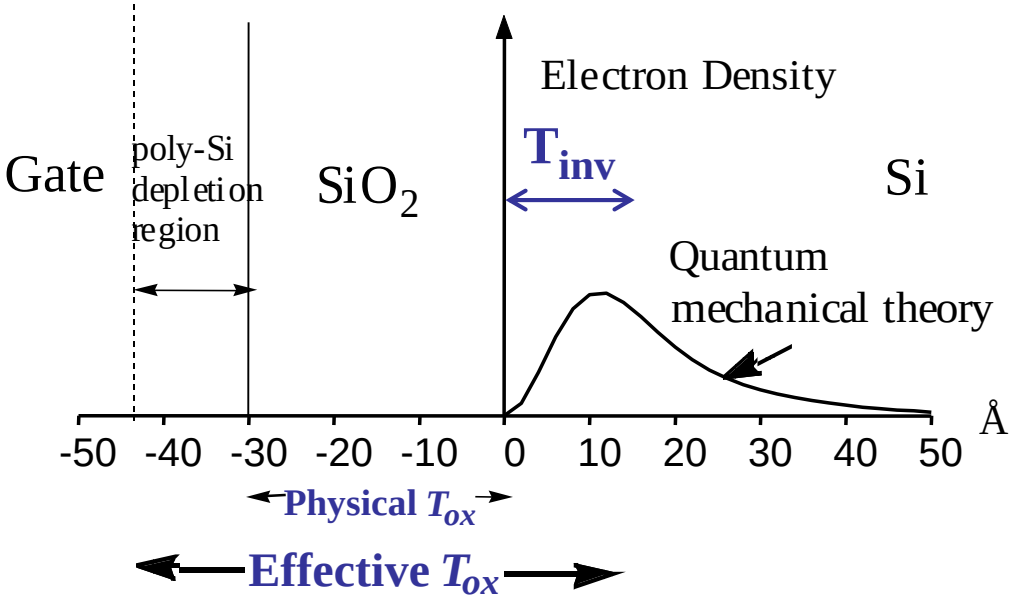
$$V_{fb} = \frac{E_g}{q} - \frac{kT}{q}\ln\left(\frac{N_c}{N_d}\right) = 1.1\,\text{V} - 0.15\,\text{V} = 0.95\,\text{V}$$

$$V_g = 0.95\,\text{V} - 0.85\,\text{V} - 1\,\text{V} - 0.11\,\text{V} = -1.01\,\text{V}$$

Is the loss of 0.11 V from the 1.01 V significant?

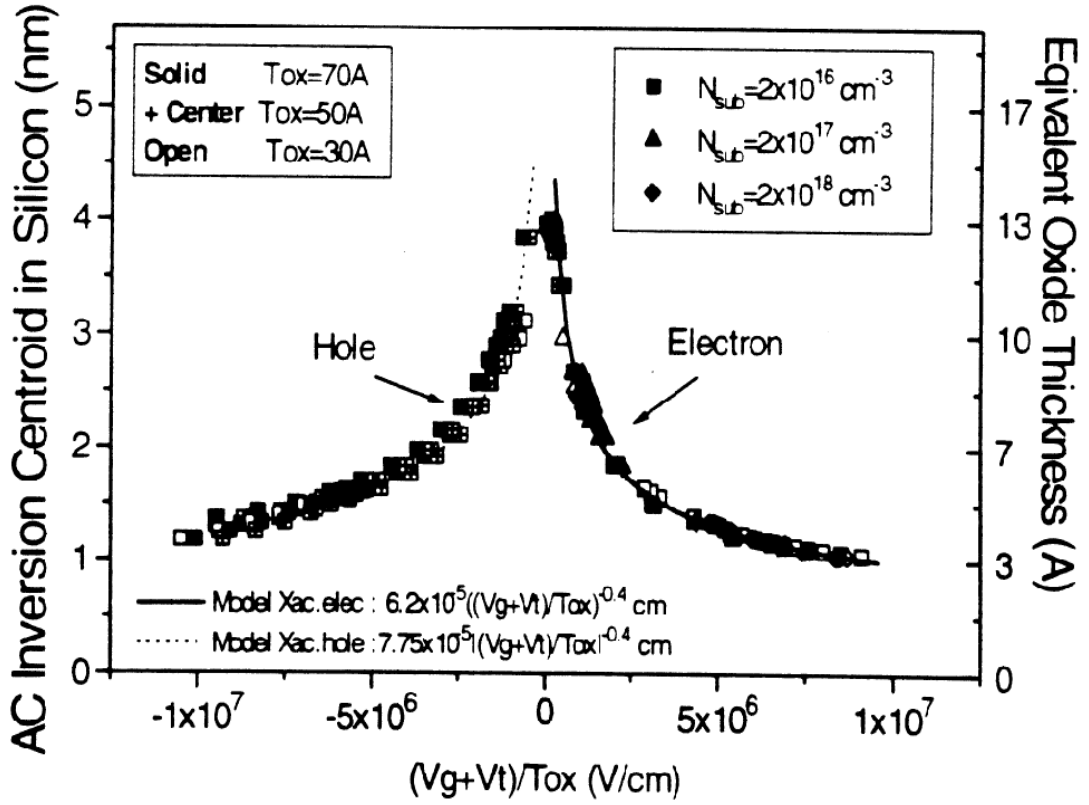
5.9 Inversion and Accumulation Charge-Layer Thickness–Quantum Mechanical Effect

Average inversion-layer location below the Si/SiO_2 interface is called the ***inversion-layer thickness,*** T_{inv} .



$n(x)$ is determined by Schrodinger's eq., Poisson eq., and Fermi function.

Electrical Oxide Thickness, T_{oxe}



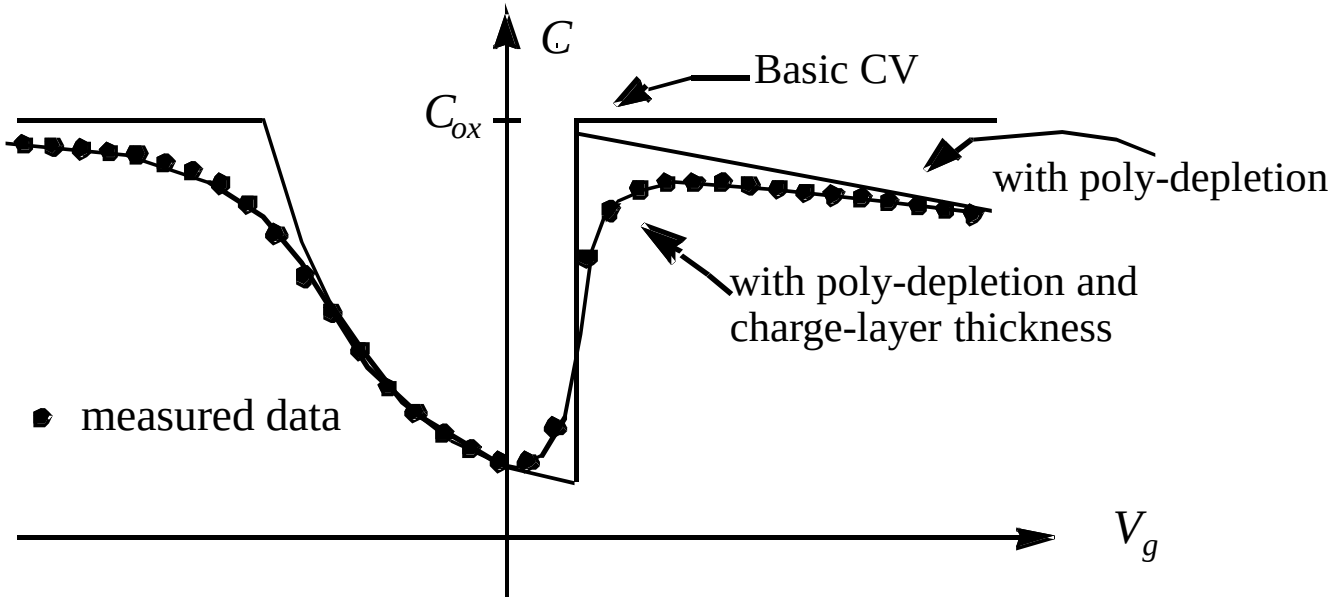
- T_{inv} is a function of the average electric field in the inversion layer, which is $(V_g + V_t)/6T_{ox}$ (Sec. 6.3.1).
- T_{inv} of holes is larger than that of electrons because of difference in effective mass.
- **T_{oxe} is the electrical oxide thickness.**

$$T_{oxe} = T_{ox} + W_{dpoly}/3 + T_{inv}/3 \quad \text{at } V_g = V_{dd}$$

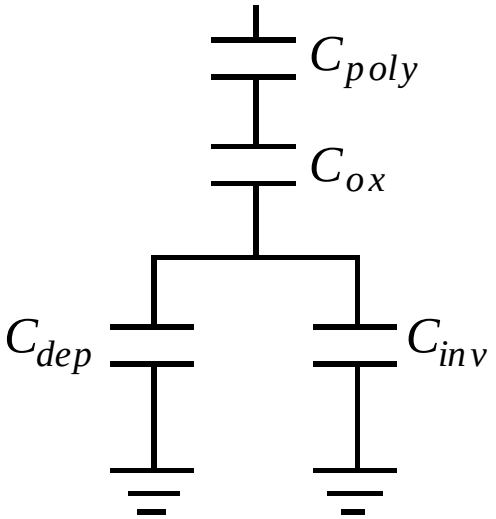
Effective Oxide Thickness and Effective Oxide Capacitance

$$Q_{inv} = C_{oxe}(V_g - V_t)$$

$$T_{oxe} = T_{ox} + W_{dpoly}/3 + T_{inv}/3$$

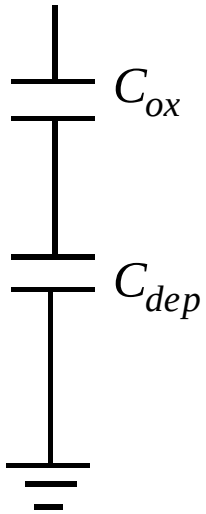


Equivalent circuit in the depletion and the inversion regimes



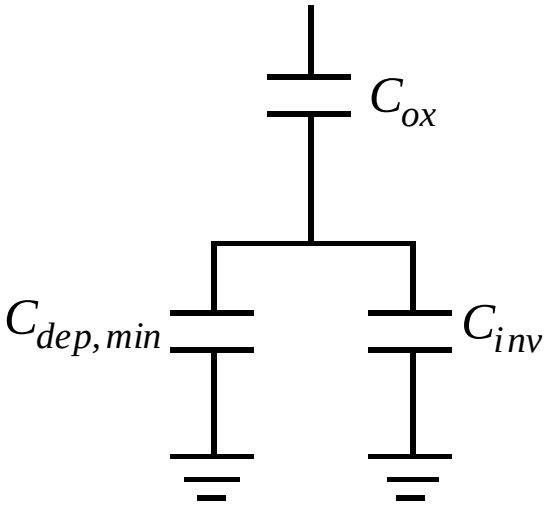
(a)

General case for both depletion and inversion regions.



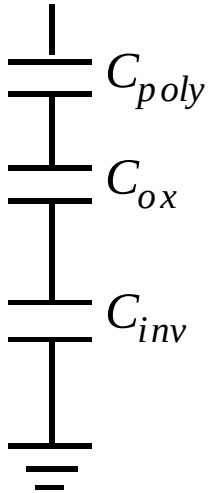
(b)

In the depletion regions



(c)

$V_g \approx V_t$

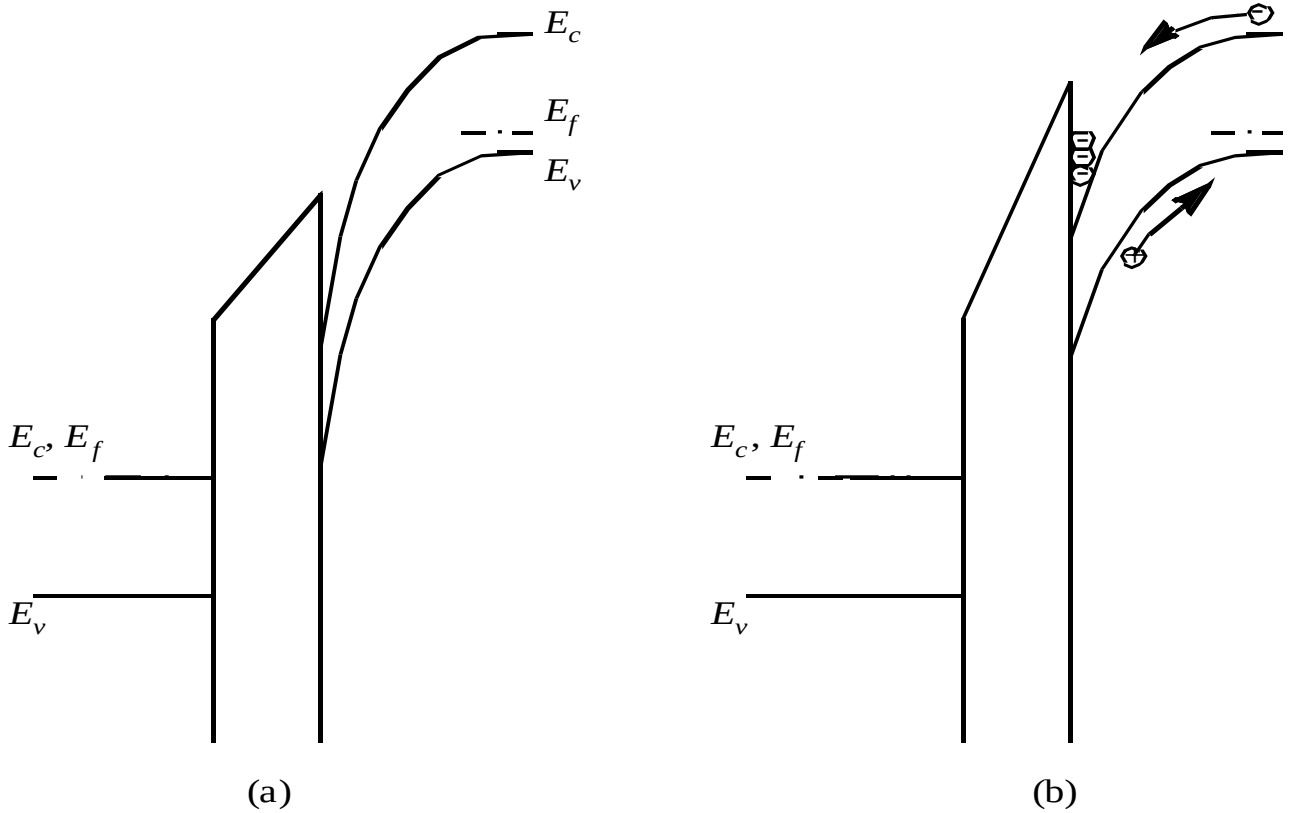


(d)

Strong inversion

5.10 CCD Imager and CMOS Imager

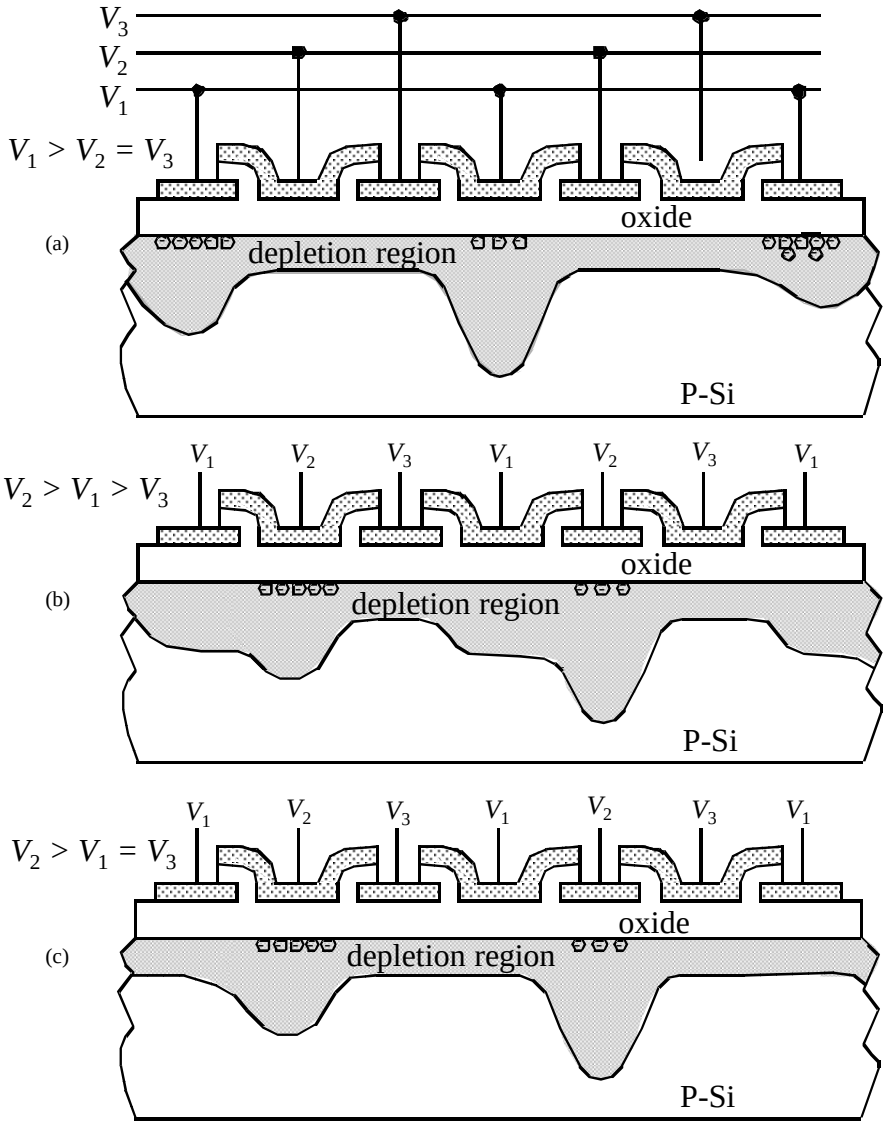
5.10.1 CCD Imager



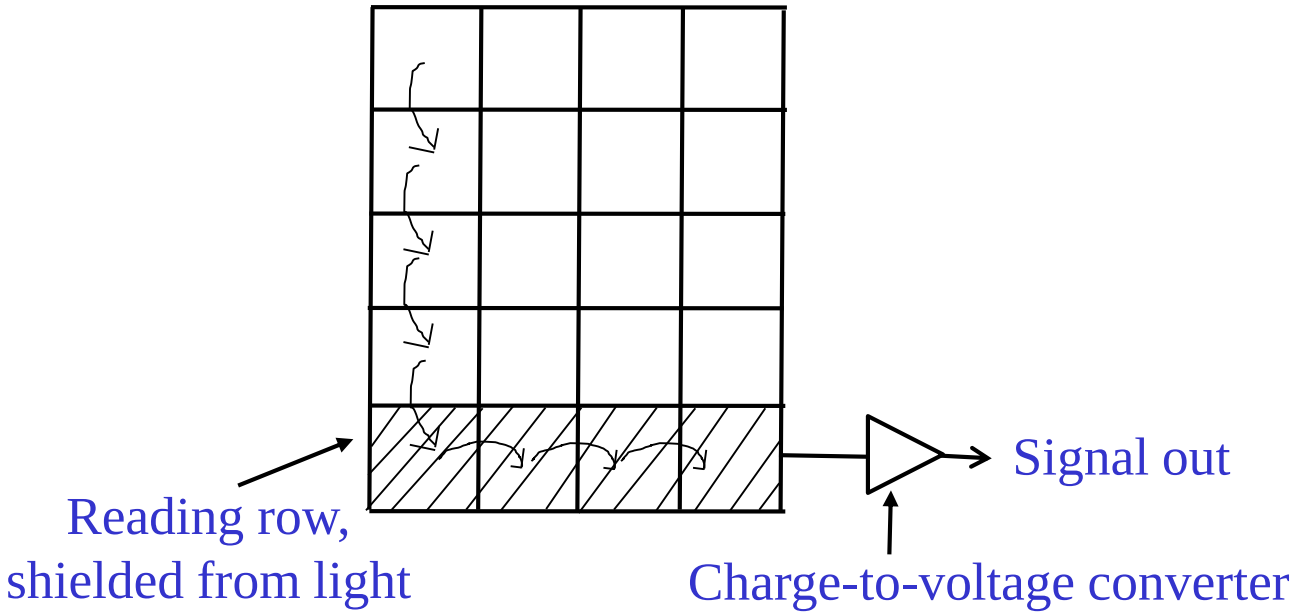
Deep depletion, Q_{inv}= 0

Exposed to light

CCD Charge Transfer

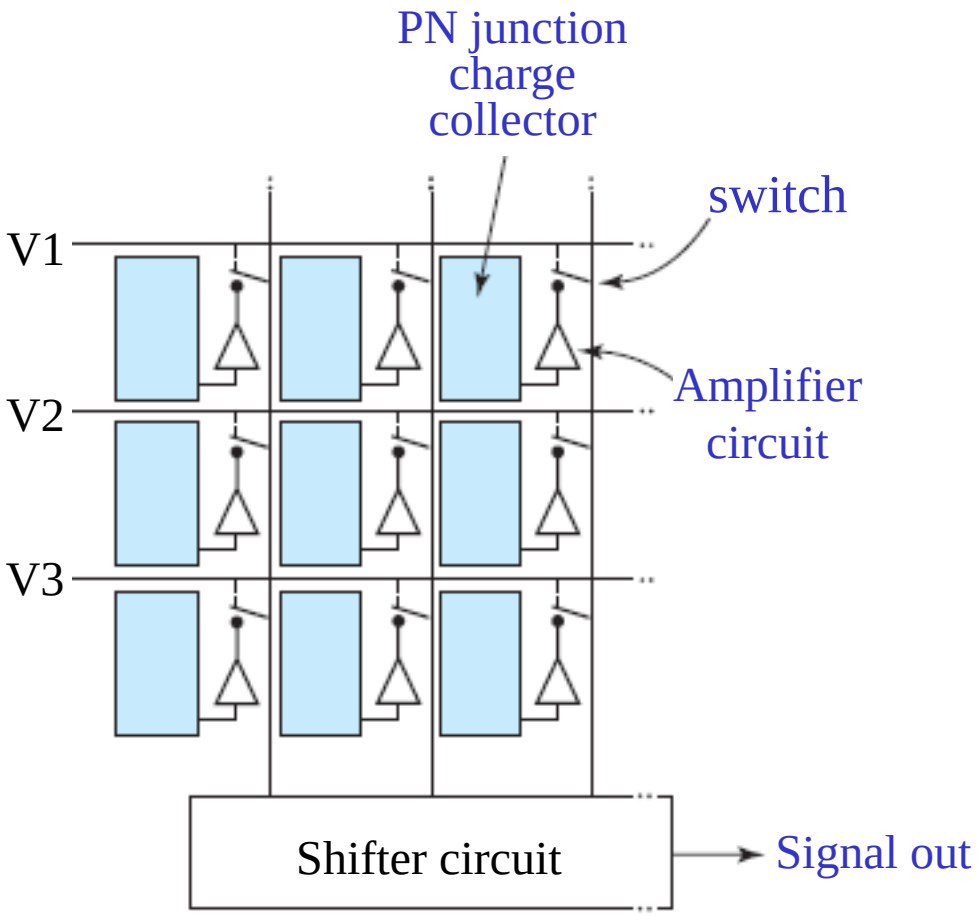


two-dimensional CCD imager



The reading row is shielded from the light by a metal film.
The 2-D charge packets are read row by row.

5.10.2 CMOS Imager



CMOS imagers can be integrated with signal processing and control circuitries to further reduce system costs. However, The size constrain of the sensing circuits forces the CMOS imager to use very simple circuits

5.11 Chapter Summary

N-type device: N^+-polysilicon gate over P-body

P-type device: P^+-polysilicon gate over N-body

$$V_{fb} = \psi_g - \psi_s + (-Q_{ox} / C_{ox})$$

$$V_g = V_{fb} + \phi_s + V_{ox} + \phi_{poly}$$

$$= V_{fb} + \phi_s - Q_s / C_{ox} + \phi_{poly}$$

5.11 Chapter Summary

$$\phi_{st} = \pm 2\phi_B \quad \text{or} \quad \pm(\phi_B + 0.45\,\text{V})$$

$$\phi_B = \frac{kT}{q} \ln \frac{N_{sub}}{n_i}$$

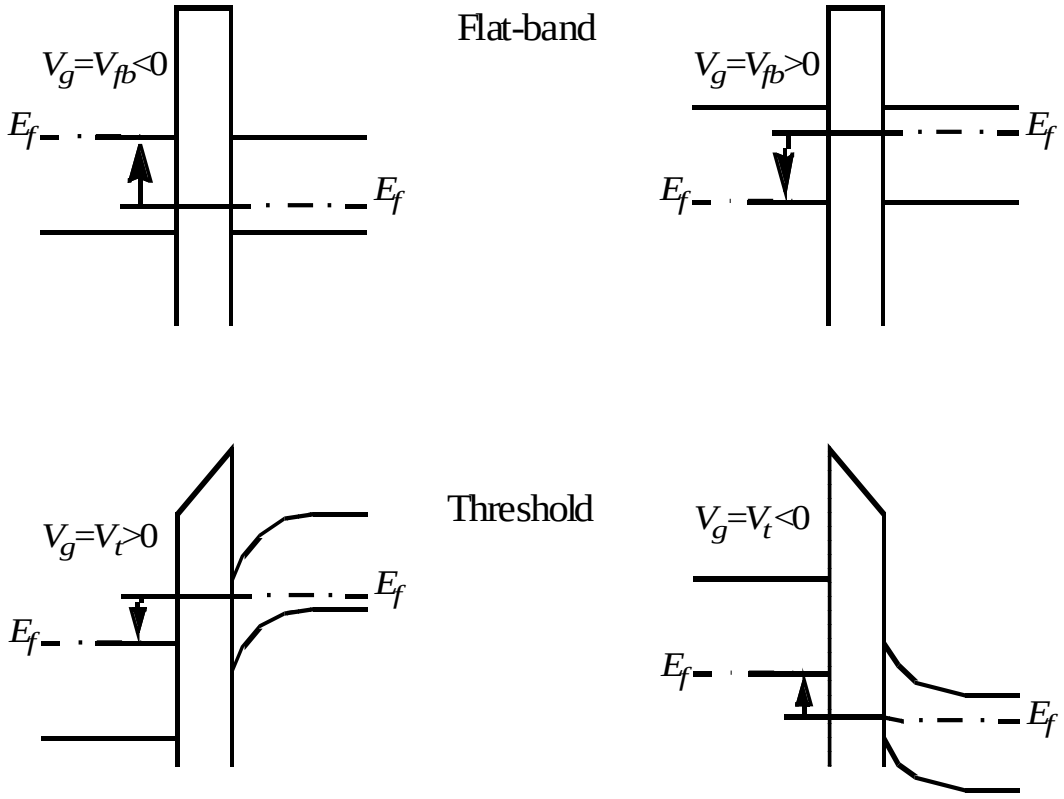
$$V_t = V_{fb} + \phi_{st} \pm \frac{\sqrt{qN_{sub}\,2\varepsilon_s\,|\phi_{st}|}}{C_{ox}}$$

+ : N-type device, – : P-type device

5.11 Chapter Summary

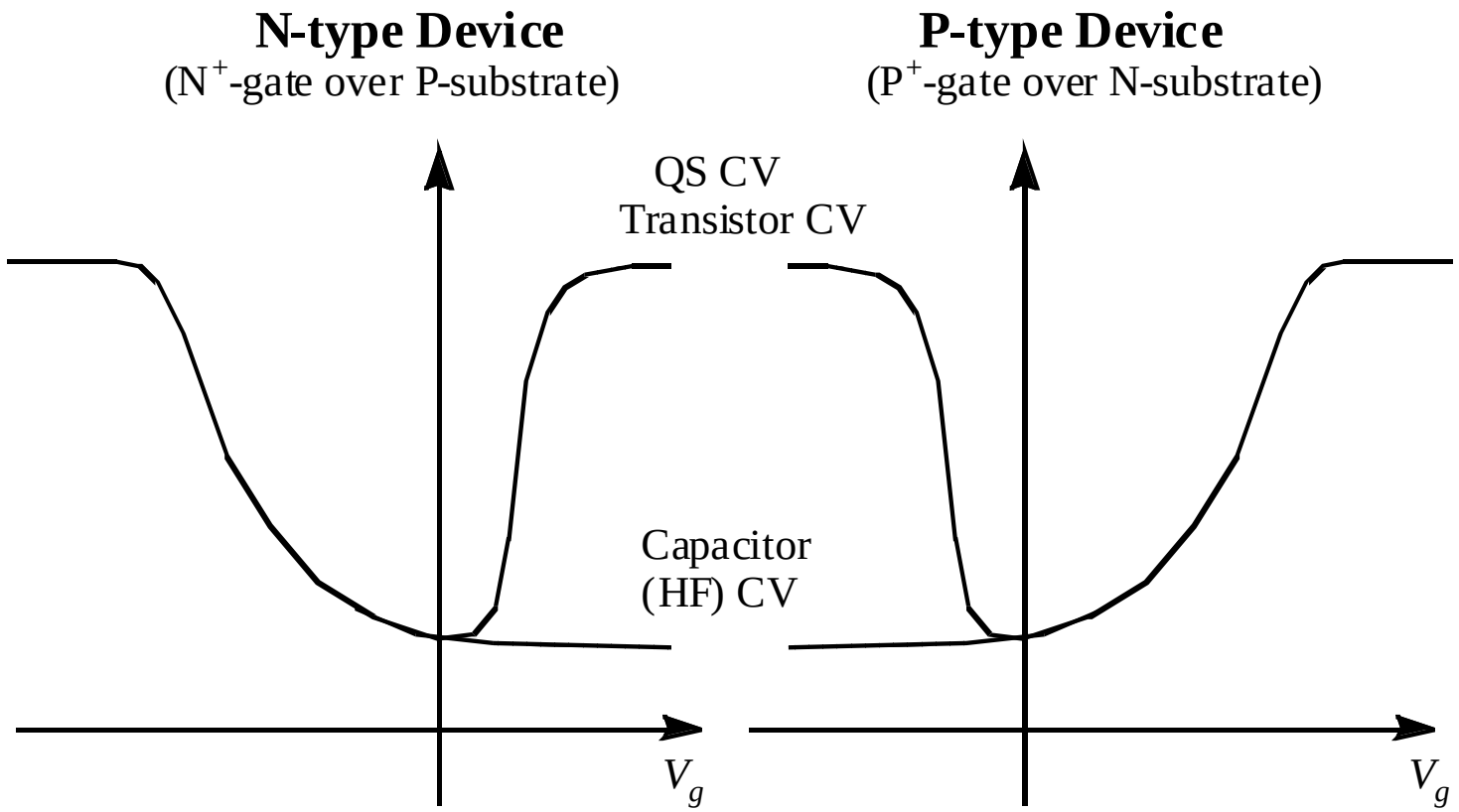
N-type Device (N^+-gate over P-substrate)

P-type Device (P^+-gate over N-substrate)



What's the diagram like at $V_g > V_t$? at $V_g = 0$?

5.11 Chapter Summary



What is the root cause of the low *C* in the HF CV branch?